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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 363 030 A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 89309317.9

(51) Int. Cl.5: G09G 3/34 , G02F 1/167

(22) Date of filing: 13.09.89

(30) Priority: 03.10.88 US 252598

(43) Date of publication of application:
11.04.90 Bulletin 90/15

(84) Designated Contracting States:
BE DE FR GB IT NL SE

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(54) Apparatus and methods for pulsing the electrodes of an electrophoretic display for achieving faster display operation.

(57) There is described a method and apparatus for driving an electrophoretic display during a writing mode. During this mode the cathodes that are not being written into are pulsed in regard to the pulsing of a grid that is being written into. The grid that is being written into is associated with a cathode line which line is caused to assume a writing mode for a longer duration than the pulse applied to the writing grid. At the same time cathode lines which are not being written into are pulsed for a time duration equivalent to the time duration of the writing grid pulse. By pulsing the electrodes in the manner described above, one increases the writing speed of the electrophoretic display while maintaining a bright uniform background for the display.

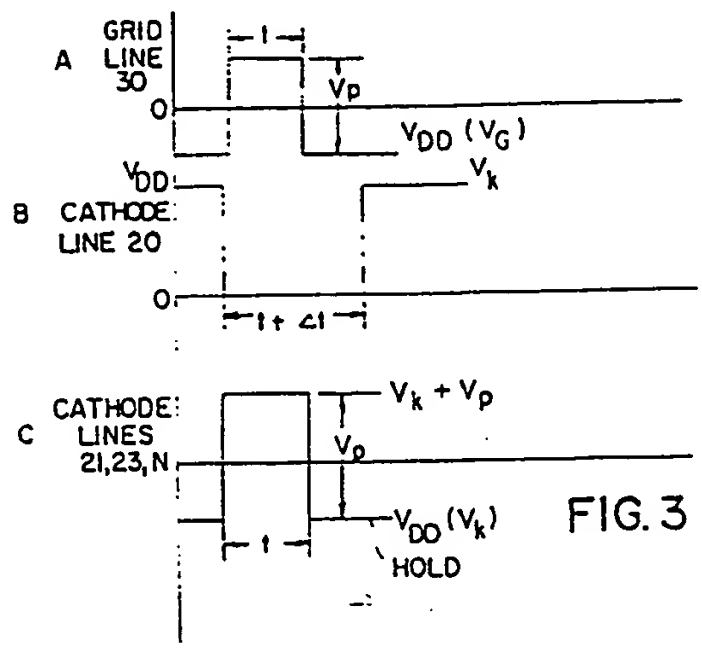

FIG. 3

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APPARATUS AND METHODS FOR PULSING THE ELECTRODES OF AN ELECTROPHORETIC DISPLAY FOR ACHIEVING FASTER DISPLAY OPERATION

BACKGROUND OF THE INVENTION

This invention relates to electrophoretic display devices in general and more particularly to an apparatus and method for pulsing the electrodes of such a display to enable enhanced speed operation of the display.

As one will ascertain, the electrophoretic effect as employed in display devices is known in the prior art. Basically, the electrophoretic effect operates on the principle that certain particles will become electrically charged and because of being electrically charged these particles can migrate from a like charged surface to an opposite charged surface. Hence, particles which become positively charged will migrate towards a negative surface or terminal or vice versa. As indicated, this effect is well known and display devices have been fabricated utilizing this effect.

For typical examples, reference is made to U.S. Patent No. 4,732,830 issued on March 22, 1988 and entitled "Electrophoretic Display Panels and Associated Methods" to Frank J. Disanto and Denis A. Krusos, the inventors herein, and assigned to Copytele, Inc., the assignee herein. Reference is also made to U.S. patent No. 4,655,897 issued on April 7, 1987 to Frank J. Disanto and Denis A. Krusos, and entitled "Electrophoretic Display Panels and Associated Methods" and also assigned to Copytele, Inc. Reference is also made to U.S. Patent No. 4,746,917 issued on May 24, 1988 to Frank J. Disanto and Denis A. Krusos, and entitled "Method and Apparatus for Operating an Electrophoretic Display Between a Display and Non-Display Mode".

The above patents give detailed descriptions of the fabrication of such displays as well as the biasing and operation of such displays to enable the electrophoretic effect to be utilized in the production of typical display panels.

In any event, if reference is made to the above noted patents, one will see that such cells or electrophoretic displays essentially contain an anode, a cathode and a grid electrode which grid electrode further controls the transportation of charged particles. In operation, the charged particles are transferred and forced against one electrode, as the anode or cathode under the influence of an applied electric field, so that the viewer may view the color of the pigment which forms a desired display pattern. In this manner the grid electrode is employed to enable control of the migration of such particles. It is also indicated that when the polarity of the field is reversed, the pigment particles are transported and packed on the opposite electrode. This is indicative, for example, of an erasing mode.

As will be further explained, the normal voltages on a typical electrophoretic panel enable the following conditions of operation. The panel can be operated in an Erase Mode where the anode electrode is negative with respect to the cathode electrode which is positive. In this mode the grid electrodes are at a low potential which is equivalent for example to a binary 0. In a Hold Mode the anode is positive, the cathodes are positive and the grid electrodes are essentially at zero voltage or at binary 0 level. As one can understand, the cathode operates between zero and positive voltages while the grid operates between low ("0") and high relates ("1").

As indicated above, a low condition will be indicated by a binary 0 and a high condition is indicated by a binary 1. In any event, during a Write Mode the anode is positive, the cathodes that are being written into are at zero potential and the grids, which are the writing grids, are at a positive or high potential as a binary 1. During this mode all non-writing cathodes are positive and non-writing grids are at low potential or more negative than the cathode.

In any event, as the prior art was aware of, in order to write at reasonable speeds the grid, during the writing mode, should be held at a positive potential or a high potential which is designated as a binary 1. As one will further understand, by making the grid potential positive one also operates to decrease the background brightness and causes some overwriting in areas where a grid set to 1 intersects a positive cathode line. This will be further explained in conjunction with the specification. In any event, as one will ascertain, the display is formulated by a means of intersecting parallel lines which are insulated from each other. These lines form an XY matrix or an XY array and consist of grid lines and cathode lines arranged in a matrix. Hence, to access any particular point in a matrix, one must have an X and a Y address. The X and Y address is indicated by one grid line and one cathode line which intersect to form a pixel point or area and which point or area is written by causing pigment particles to migrate out of that pixel area on said display.

At the intersection of the X and Y addresses in the matrix, one will thereby provide a writing condition. In any event, as indicated above, when the grid potential becomes positive there is a decrease in the background brightness of the display due to the fact that the potential between the grid and

cathode has changed for non-writing lines.

In addition, and of greater consequence, a dark line will appear at the leading edge of the picture being written (corresponding to the cathode at zero potential). The black line is indicative of the fact that all the pigment has left the cathode in the pixels being written. This is desirable, however, it is also noted that when the potential of the cathode being written into is made positive, some of the pigment returns to the cathode resulting in incomplete writing and poor contrast. It is believed that this effect is probably due to the fact that the negatively charged pigment, which has only gone a short distance beyond the grid, is attracted back to the cathode by the combined positive grid and cathode fields. These factors substantially decrease the writing speed of such a display and provide a lack of contrast and so on, as described above.

It is the object of the present invention to apply selectable pulses to the grid and cathode electrodes during a write mode whereby the pulses supplied will serve to maintain the grid to cathode potential of non-writing electrodes at a fixed value which is indicative of a good contrast level. At the same time, a writing pulse applied to the grid remains for a given duration while the cathode to be written is held low for a longer duration. In this manner, one will have a positive grid potential at the start of writing a given pixel and a negative grid (which will repel the pigment that has traveled to the anode side of the grid) when writing of that pixel (cathode from zero to positive potential) is complete. In this manner, as will be explained, the effective speed of operation of the display is dramatically increased and results in a speed increase of approximately 6:1 over a conventional display operated according to the teachings of the prior art.

It is further indicated that the apparatus and method to be provided also pulses all cathodes which are not being written by a pulse of the same nature as the writing grid pulse. In this manner, the potential between the nonwriting cathode lines and the grid lines remains constant and hence the above-noted problems are avoided.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENT

Apparatus for driving an electrophoretic display in a write mode, which display is of the type having a plurality of grid lines insulated from a plurality of cathode lines with said grid and cathode lines positioned perpendicular to one another to provide an X-Y matrix. Said display having an anode electrode, said display enabling a picture to be displayed on said cathode by selectively accessing intersecting grid and cathode lines each indicative of a pixel and varying the bias between said lines to cause said particles to migrate to said anode for each selected intersection. The improvement in connection therewith comprising means coupled to said grid lines to provide a grid pulse on said lines, to be written of a given duration and of a given polarity and amplitude indicative of a write bias for said grid lines, means coupled to a selected intersecting cathode line associated with said grid line and selected according to a pixel to be written to provide a cathode pulse to said cathode line of an opposite polarity to said grid pulse and commencing at the start of said grid pulse but having a longer duration than said given duration whereby said cathode pulse is present when said grid pulse terminates. Apparatus for pulsing all non-writing cathodes with a pulse of the same amplitude and duration as the grid pulse.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simple schematic view depicting an electrophoretic display according to this invention.

FIG. 2 is a schematic diagram showing an XY matrix array consisting of intersecting grid and cathode lines as provided in the electrophoretic display.

FIG. 3(A-C) is a series of timing diagrams showing the pulsing techniques according to this invention.

FIG. 4 is a schematic diagram showing a grid drive amplifying circuit employed in conjunction with this invention.

FIG. 5 is a schematic diagram showing a cathode drive amplifying circuit according to this invention.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring to FIG. 1 there is shown a simple schematic diagram necessary to indicate operation of a typical electrophoretic display. The reference numeral 11 refers to a cathode electrode which, as one will see from the above noted patents, is one of a number of a series of lines which are arranged, for example, in the horizontal or X direction. Each of these lines, as cathode lines, can be accessed or biased by means of a separate voltage applied to such a line. The associated grid lines are represented by reference numeral 12. Each grid structure, four of which are shown in FIG. 1, is insulated from the cathode lines by means of an insulator layer 13. The plate, or anode electrode, is referenced in FIG. 1 by reference numeral 15. In order to access a point on the matrix a

potential is applied between the grid and cathode lines. This potential will access an intersection point in the X-Y matrix indicative of a pixel. In any event, the electrophoretic dispersion 16, which is located between the anode and cathode, contains a plurality of submicron pigment particles which can be charged according to known techniques.

The grid array, as indicated, overlies the cathode array and is insulated therefrom. When a given potential is applied between an X and Y point in the matrix, electrophoretic particles which are within the vicinity of the intersection between the grid and cathode structures are accelerated towards the anode. Particles, as 17 and 18, as indicated by the arrows, deposit on the plate or anode electrode and remain there until the charge or bias is reversed.

As one can ascertain from the above described prior art, the movement of the particles, as controlled by the intersection between an X and a Y line, causes these particles to migrate towards the anode. Thus, if the grid to cathode potential is properly selected, electrophoretic particles which are negatively charged will be attracted towards the positive anode 15 which will assume the color of the pigment particles.

An image is formed on the cathode. The cathode image being a dark color, which is the color of the suspension medium in which the particles are suspended. As one can understand, the pigment particles are suspended in an electrophoretic dispersion and essentially are yellow particles in certain embodiments with the dispersion medium having a dark blue color. Thus, by viewing the cathode surface, either a yellow image on a dark blue background or a dark blue image on a yellow background may be viewed.

Referring to FIG. 2 there is shown a top view of a typical X-Y matrix consisting of cathode lines which are arranged in the horizontal plane and grid lines which are perpendicular to the cathode lines and which are insulated therefrom. Thus, referring to FIG. 2, there is shown four cathode lines designated as 20, 21, 22 and N. It is of course understood that the number of cathode lines in the Y direction may consist of hundreds or thousands, depending upon the size of the display.

As indicated, insulated from the cathode lines and perpendicular thereto, there are shown four grid lines 30, 31, 32 and X. It is also indicated that there can be many more grid lines associated with a typical display.

As seen in FIG. 2, each cathode line has a suitable driving amplifier circuit shown in modular form and indicated by reference numerals 40, 41, 42 and 43. In a similar manner, each grid line has a suitable driving amplifier referenced by modules 50, 51, 52 and 53. The driving signals for the grid and cathodes are obtained by typical driving generators as 60 and 61. As will be explained, these generators are such that they will provide the type of pulses necessary for the improved operation, as will be described in conjunction with the timing diagrams.

As indicated above, the display can typically be operated in an Erase Mode, a Hold Mode or a Writing Mode. In the Erase Mode the anode electrode, which is not shown in FIG. 2, is placed at a negative potential while the cathodes as lines 20-N are operated at a positive potential. In this mode the grid lines as 30 to X are operated at a low potential such a negative potential designated as zero for purposes of this discussion. In the hold mode the anode is positive while the cathodes are held positive and the grids are again at a low potential. As one can understand from the above, the cathode operates between zero and positive voltages. The grid operates between low and high voltages and for purposes of the present discussion a low will be indicative of zero and a high would be indicative of a 1.

In the Write Mode, the anode is held positive while cathode lines which are being written are placed at zero potential while non-writing cathodes are placed at positive potential. This is the same potential as employed in the Hold Mode. In this manner the writing grids are operated at a high potential and the non-writing grids are operated at the low potential or zero potential: This is exactly what the prior art taught in order to achieve the writing operation.

Based on prior art operation and looking at FIG. 2, the following problems occur. First let us assume that one desires to write at the intersection of cathode line 20 with grid line 30. In this manner grid line 30, via the driver amplifier 50, would be placed at the high or positive level. The cathode line 20, by means of the driver amplifier 40, would be set to a zero or ground potential. All other cathode lines, as 21, 23 and N would be set at a positive potential while all other non-writing grids, such as 31, 32 and X, would be set at the low potential. When the grid 30 has a positive potential applied thereto, an overwriting occurs between the intersections of grid 30 and cathode lines 21, 23 and N. As one can ascertain, the existence of the positive potential on the grid line 30 changes the cathode to grid voltage for lines 21, 23 and N. This causes an overwriting in each of these areas. This overwriting, essentially, reduces the effective contrast of the display.

In addition, and as indicated above, a dark line appears at the leading edge of the picture being written which corresponds to the cathode line 20 being at zero potential. Hence when the grid 30 is made positive a black line or an extremely black area appears at the intersection of cathode line 20

and grid line 30. This black line is indicative of the fact that all the pigment has left the cathode in the indicated area intersection between grid line 30 and cathode line 20. In any event, when the potential of the cathode line 20, which is being written, is made positive some of the pigment returns to the cathode area resulting in incomplete writing and poor contrast. As indicated above, this is probably due to the fact that the negatively charged pigment, which has only gone a short distance beyond the grid electrodes, is attracted back to the cathode by the combined positive grid and cathode fields. The amount returned is a function of writing speed.

Thus, as will be explained, in order to solve this problem it is indicated that the amplifiers as for example 50, 51, 52 and 53 will be operated so that there is a positive grid potential at the start of writing a given pixel and a negative grid potential which will repel the pigment that has traveled to the anode side of the grid when writing of that pixel as for example when the cathode goes from zero to positive potential and therefore when the writing of that pixel is complete. Furthermore, the circuit will also operate to pulse all cathodes not being written in a positive potential direction and for a time duration exactly the same as the duration of the grid pulse. In this manner, all lines which are not being written maintain the same voltage difference between grid and cathode and hence do not degrade the brightness of the non-written areas. The cathode line that is being written is pulsed from a positive to a zero value for a duration longer than the duration of the grid pulse. In this manner the above-described problems have been substantially reduced.

For examples of typical timing diagrams, reference now will be made to FIG. 3. FIG. 3 shows the necessary timing relationships and waveforms for pulsing the grid and cathode electrodes according to the teachings of this invention. Referring to FIG. 3 there is shown three wave forms (A, B, C) indicative of the waveforms provided by the driving amplifiers and driving generators as 60 and 61 of FIG. 2 during the write mode. Let us assume, for example, that we are about to access the intersection between cathode line 20 and grid line 30. As shown in FIG. 3A, the grid line 30 will go from a given value, called $V_{dd}(V_G)$ to a positive value, thus exhibiting a positive peak of VP and for a duration of t seconds.

The waveform of FIG. 3B shows that cathode line 20 goes from V_{DD} (V_K) which is the hold voltage to zero or ground and remains for a duration of $t + \Delta t$ or for a longer duration than the pulse applied to the grid line 30. After the duration of $t + \Delta t$ cathode line 20 returns to the level V_{DD} - (V_k). At the same time the cathode lines as 21, 23 and N which are those lines that are not being written are pulsed with a transition from the V_{DD} voltage which is the Hold voltage in a positive direction to go to a level of $V_k + V_p$ where V_p is the same as V_p in FIG. 3A. The time duration of the cathode line pulse, time t, is the same as the duration of the grid pulse of FIG. 3A.

Thus, as explained, the above waveforms prevent the above-described problems whereby the cathode to grid potential of all cathode lines which are not being written into remains the same due to the pulsing of the non-writing cathode lines as shown in FIG. 3 as well as keeping the writing cathode at ground for a longer duration than the writing grid pulse.

Thus, the writing cathode line is held at zero potential for a longer duration than the positive pulse duration applied to the writing grid and non-writing cathodes therefore preventing the above-described problem whereby charged pigment will not be attracted back to the cathode by the combined positive grid and cathode fields as would be accomplished in the prior art. It is of course understood that one can write into multiple grid lines for each cathode line. In any event, if this occurs the same pulse configuration is generated by the circuitry for each of the grid lines to be written into in regard to the single cathode line as line 20 and the pulses having the time durations as depicted in the figure are appropriate.

In a typical display the following voltages were applicable. The voltage V_G was equal to -5 volts, the voltage V_k was equal to +19 volts, the voltage pulse V_p equals the +10 volts. The hold voltage, which is V_k-V_g was 24 volts while the grid transition went from -5 volts or from V_G to +5 volts indicative of a 10 volt peak (VP). The non- writing cathode transition is from V_k equal to +19 volts to $V_k + V_p$ equal to +29 volts. The duration of the grid pulse t is dependent upon the writing time for a particular line. Essentially one can write one line in 4 milliseconds whereby t would approximately equal 3 milliseconds with Δ t equal to 1 millisecond.

In a similar manner, if one had a maximum writing time say of 10 milliseconds or more, t would be equal to 7 or 8 milliseconds while Δ t would be 2 or 3 milliseconds or more. It is indicated that for writing times which exceed 10 milliseconds the duration of pulse t would stay at 7 or 8 milliseconds while the remaining time, Δ t, would vary accordingly.

Referring to FIG. 4 there is shown a typical grid driving amplifier such as employed for amplifiers 50, 51, 52 and 53. Essentially the amplifier has an input to driver 60 which is synchronous to the cathode scan and of a suitable width as described above in FIG. 3. It should be apparent to those skilled in the art that there are many techniques available for providing such pulses which are es-

sentially as shown in FIG. 3.

The output of the driver 60 is coupled to a potentiometer 62 which is suitably biased and serves as the input to the operational amplifier 61 which also has a biasing adjustment coupled thereto. The potentiometers 62 and 63 are utilized to set the effective DC levels which are applied to the grid in regard to the pulse as shown for example in FIG. 3A.

In regard to FIG. 4 the driver stage 60 is implemented using an 7407 while the operational amplifier 61 is an MC4741. The driving amplifier is a DC amplifier to maintain the grid lines at a suitable level when writing does not occur.

Referring to FIG. 5 there is shown a schematic of the DC cathode amplifiers as for example amplifiers 40, 41, 42 and 43 of FIG. 2. Each cathode amplifier has a driver input stage 70 which receives an input the same as the input to driver 60 in FIG. 4. The output of the driver 70 is coupled via a potentiometer 71 to the input of an operational amplifier 72 which also has its biasing adjusted by means of potentiometer 73. In this manner the output of the operational amplifier 72 is implemented to provide the pulse and DC levels as shown and necessary to drive the corresponding cathode lines as indicated in FIGS. 3B and C.

In regard to the schematic shown in FIG. 5, the inverter is also a 7404 integrated circuit while the operational amplifiers is an LM-2900. In view of the above, it should be apparent to those skilled in the art that the technique of driving the grid and cathode lines as described above enables faster display operation while circumventing many of the problems indicated above as associated with prior art displays and driving techniques.

Claims

1. An electrophoretic matrix display (Fig. 2) having:
a multiplicity of addressable intersections formed between a plurality of grid electrodes (30; 31; X) and a plurality of cathodes (20; 21; ....; N);
grid address means (60, 50, 51, ...; 53) coupled to the plurality of grid electrodes (30) 31, ..., X) and arranged to apply a grid pulse (A) to a selected one (30) thereof; and,
cathode address means (61, 40, 41, ..., 43) coupled to the plurality of cathodes (20, 21, ... N) and arranged to apply a cathode pulse (B) to a selected one (20) thereof thereby to establish a write bias at an addressed intersection formed between the selected grid electrode (30) and the selected cathode (20);
characterised in that
the cathode address means (61, 40 41, ..., 43) is adapted to apply the cathode pulse (B) for a duration (t + Δt) that is larger than that (t) for the grid pulse (A) and such that it (B) shall persist (Δt) following termination of the grid puise (A).

2. A display, as claimed in claim 1, wherein the grid address means (60, 50, 51,..., 53) is arranged to apply the grid pulse (A) for a duration (t) of between 3 and 8 milliseconds; and
the cathode address means (61, 40, 41,..., 43) is adapted to apply the cathode pulse (B) for a duration (t + Δt) of between 4 and 20 milliseconds.

3. A display, as claimed in either preceding ciaim 1 or claim 2,
further characterised in that:
the cathode address means (61, 40, 41, ..., 43) is adapted to apply an additional cathode pulse (C) to each remaining cathode (21, 23, ... N) thereby to reduce any change in a predetermined bias between each remaining cathode (21, 23, ..., N) and the selected grid electrode (30) when the grid pulse (A) is applied.

4. An electrophoretic matrix dispiay (Fig. 2) having:-
a multiplicity of addressable intersections formed between a plurality of grid electrodes (30; 31; X) and a plurality of cathodes (20; 21;....; N);
grid address means (60, 50, 51, ..., 53) coupled to the plurality of grid electrodes (30, 31, ..., X) and arranged to apply a grid pulse (A) to a selected one (30) thereof; and,
cathode address means (61, 40, 41, ..., 43) coupled to the plurality of cathodes (20, 21, ..., N) and arranged to apply a cathode pulse (B) to a selected one (20) thereof thereby to establish a write bias at an addressed intersection formed between the selected grid electrode (30) and the selected cathode (20);
Characterised in that:
the cathode address means (61, 40, 41, ... 43) is adapted to apply an additional cathode pulse (C) to each remaining cathode (21, 23, ... N) thereby to reduce any change in a predetermined bias between each remaining cathode (21, 23, ..., N) and the selected grid electrode (30) when the grid pulse (A) is applied.

5. A display, as claimed in either preceding claim 3 or claim 4, wherein
the grid address means (60, 50, 51, ..., 53) and the cathode address means (61, 40, 41, ..., 43) are adapted to co-operate such that the grid pulse (A) and each additional cathode pulse (C) are coincident, and of the same polarity sense and magnitude (Vp) that the predetermined bias between the selected grid electrode (30) and each remaining cathode (21, 23, ..., N) shall in each case be maintained constant when the grid pulse (A) is applied.

6. A method of operating an electrophoretic

matrix display wherein:
a grid pulse is applied to a selected grid electrode; and
a cathode pulse is applied to a selected cathode to establish a write bias at an addressed intersection formed between the selected grid electrode and the selected cathode;
characterised in that
the cathode pulse is applied for a longer duration than the grid pulse so that the selected cathode is maintained at a pulse level after the grid pulse has terminated.

7. A method, as claimed in claim 6, wherein:
the grid pulse is applied for a duration of between 3 and 8 millisecond; and
the cathode pulse is applied for a duration of between 4 and 20 milliseconds.

8. A method, as claimed in either preceding claim 6 or claim 7,
further characterised in that:
an additional cathode pulse is applied to each remaining cathode intersecting the selected grid electrode, which pulse is in each case coincident with the grid pulse and is such as to reduce any change in predetermined bias between the selected grid electrode and the remaining cathode to which it is applied when the grid pulse is applied to the selected grid electrode.

9. A method of operating an electrophoretic matrix display wherein:
a grid pulse is applied to a selected grid electrode; and
a cathode pulse is applied to a selected cathode to establish a write bias at an addressed intersection formed between the selected grid electrode and the selected cathode;
characterised in that:
an additional cathode pulse is applied to each remaining cathode intersecting the selected grid electrode, which pulse is in each case coincident with the grid pulse and is such as to reduce any change in predetermined bias between the selected grid electrode and the remaining cathode to which it is applied when the grid pulse is applied to the selected grid electrode.

10. A method, as claimed in either preceding claim 8 or claim 9, wherein:
the additional cathode pulse is in each case of the same polarity sense and amplitude as the grid pulse such that the predetermined bias between the selected grid electrode and the remaining cathode to which it is applied is maintained constant when the grid pulse is applied.

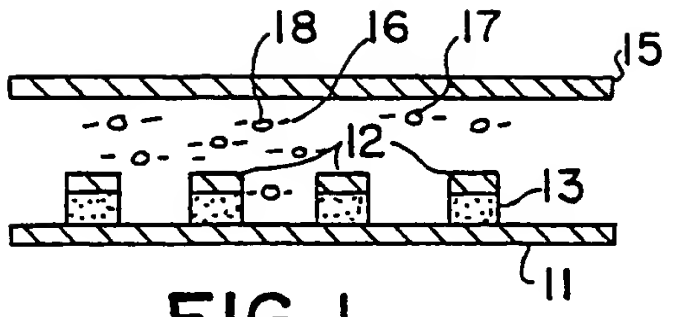
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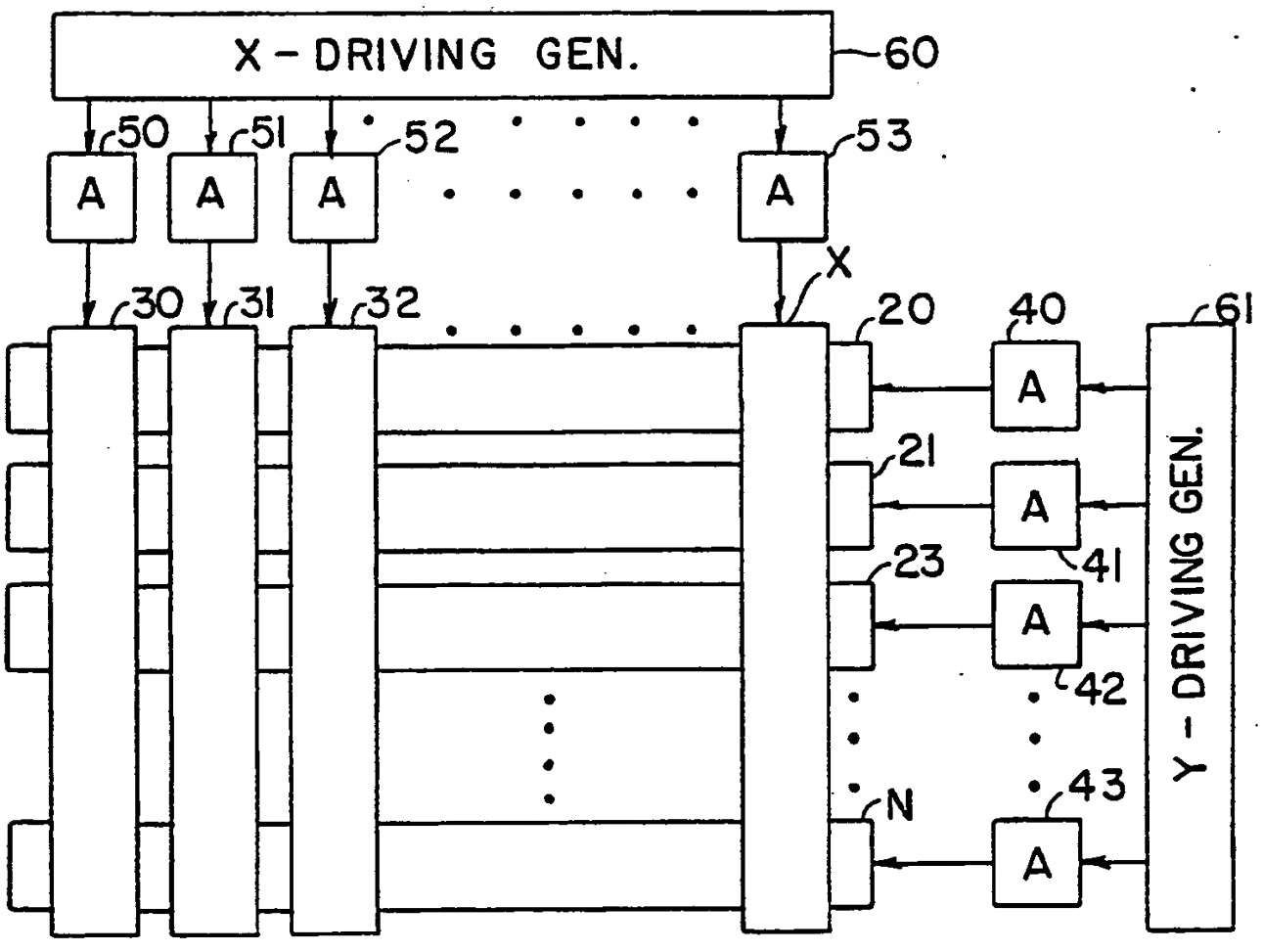
FIG. 1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60
50
51
52
53
A
30
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32
X
20
40
61
21
23
41
42
43
N
Y - DRIVING GEN.

FIG. 2

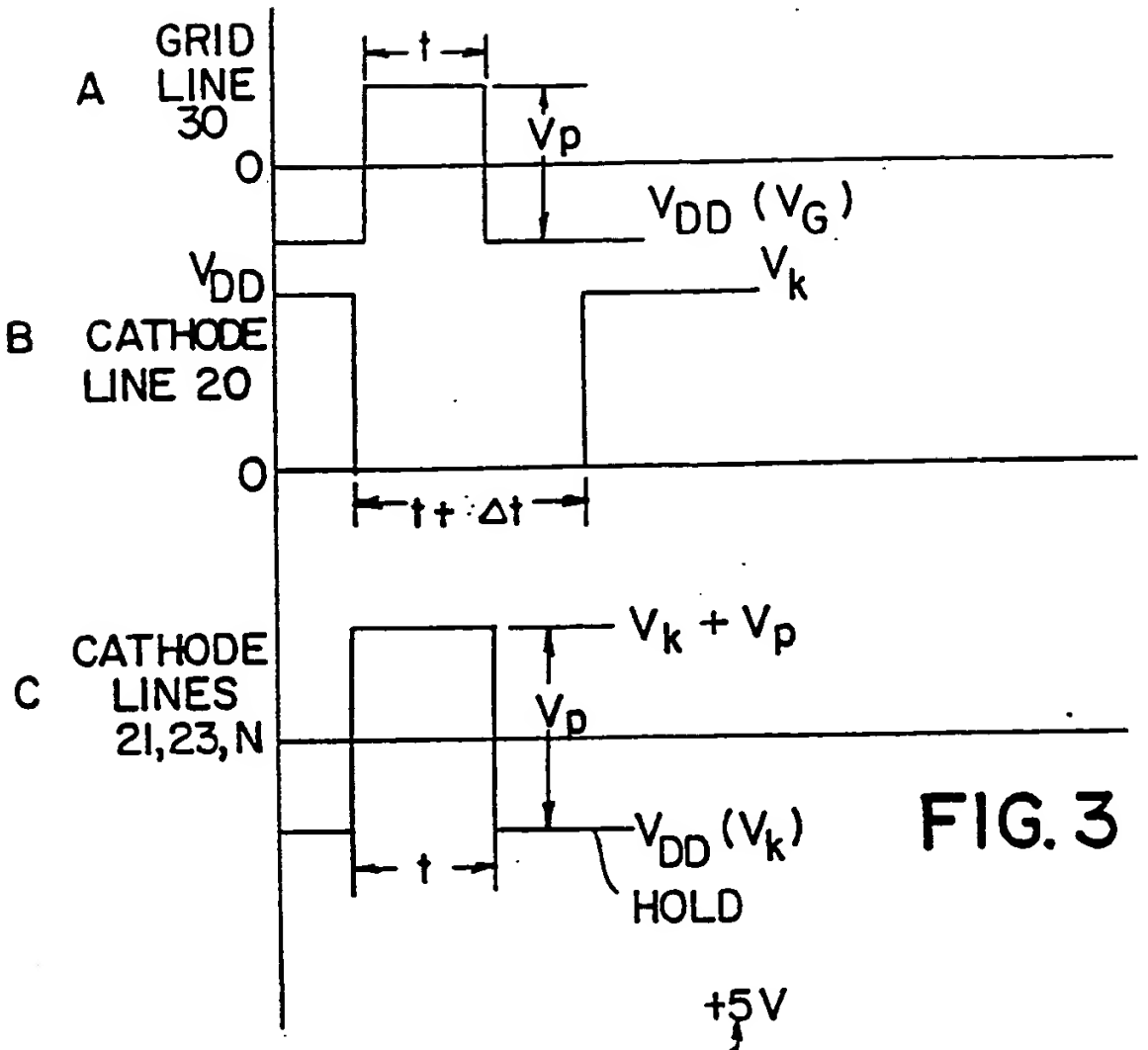

FIG. 3

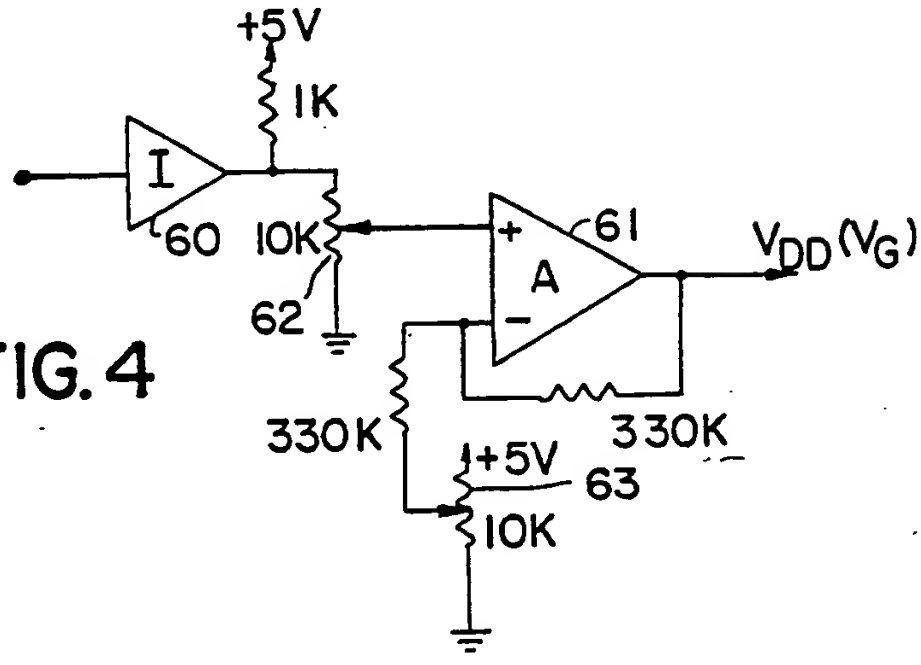

FIG. 4

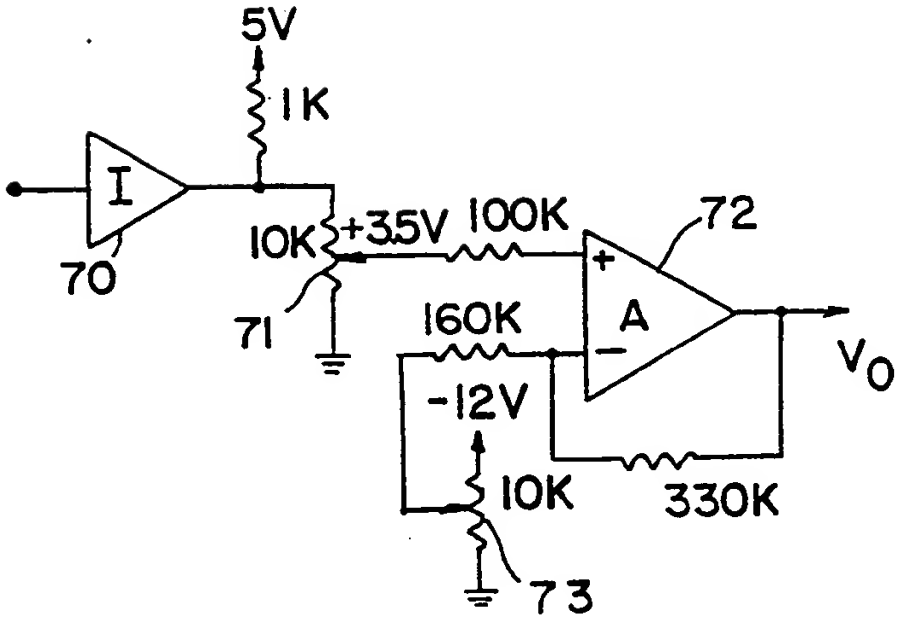

FIG. 5

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 363 030 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication of patent specification: **03.08.94**

(51) Int. Cl.5: **G09G 3/34**, G02F 1/167

(21) Application number: **89309317.9**

(22) Date of filing: **13.09.89**

(54) Apparatus and methods for pulsing the electrodes of an electrophoretic display for achieving faster display operation.

(30) Priority: **03.10.88 US 252598**

(43) Date of publication of application:
11.04.90 Bulletin 90/15

(45) Publication of the grant of the patent:
03.08.94 Bulletin 94/31

(84) Designated Contracting States:
BE DE FR GB IT NL SE

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GB-A- 2 161 308

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EP 0 363 030 B1

Description

This invention relates to electrophoretic display devices in general and more particularly to an apparatus and method for pulsing the electrodes of such a display to enable enhanced speed operation of the display.

As one will ascertain, the electrophoretic effect as employed in display devices is known in the prior art. Basically, the electrophoretic effect operates on the principle that certain particles will become electrically charged and because of being electrically charged these particles can migrate from a like charged surface to an opposite charged surface. Hence, particles which become positively charged will migrate towards a negative surface or terminal or vice versa. As indicated, this effect is well known and display devices have been fabricated utilizing this effect.

For typical examples, reference is made to U.S. Patent US-A-4,732,830 issued on March 22, 1988 and entitled "Electrophoretic Display Panels and Associated Methods" to Frank J. Disanto and Denis A. Krusos, the inventors herein, and assigned to Copytele, Inc., the assignee herein. Reference is also made to U.S. patent US-A-4,655,897 issued on April 7, 1987 to Frank J. Disanto and Denis A. Krusos, and entitled "Electrophoretic Display Panels and Associated Methods" and also assigned to Copytele, Inc. Reference is also made to U.S. Patent US-A-4,746,917 issued on May 24, 1988 to Frank J. Disanto and Denis A. Krusos, and entitled "Method and Apparatus for Operating an Electrophoretic Display Between a Display and Non-Display Mode".

The above patents give detailed descriptions of the fabrication of such displays as well as the biasing and operation of such displays to enable the electrophoretic effect to be utilized in the production of typical display panels.

In any event, if reference is made to the above noted patents, one will see that such cells or electrophoretic displays essentially contain an anode, a cathode and a grid electrode which grid electrode further controls the transportation of charged particles. In operation, the charged particles are transferred and forced against one electrode, as the anode or cathode under the influence of an applied electric field, so that the viewer may view the color of the pigment which forms a desired display pattern. In this manner the grid electrode is employed to enable control of the migration of such particles. It is also indicated that when the polarity of the field is reversed, the pigment particles are transported and packed on the opposite electrode. This is indicative, for example, of an erasing mode.

As will be further explained, the normal voltages on a typical electrophoretic panel enable the following conditions of operation. The panel can be operated in an Erase Mode where the anode electrode is negative with respect to the cathode electrode which is positive. In this mode the grid electrodes are at a low potential which is equivalent for example to a binary 0. In a Hold Mode the anode is positive, the cathodes are positive and the grid electrodes are essentially at zero voltage or at binary 0 level. As one can understand, the cathode operates between zero and positive voltages while the grid operates between low ("0") and high relates ("1").

As indicated above, a low condition will be indicated by a binary 0 and a high condition is indicated by a binary 1. In any event, during a Write Mode the anode is positive, the cathodes that are being written into are at zero potential and the grids, which are the writing grids, are at a positive or high potential as a binary 1. During this mode all non-writing cathodes are positive and non-writing grids are at low potential or more negative than the cathode.

In any event, as the prior art was aware of, in order to write at reasonable speeds the grid, during the writing mode, should be held at a positive potential or a high potential which is designated as a binary 1. As one will further understand, by making the grid potential positive one also operates to decrease the background brightness and causes some overwriting in areas where a grid set to 1 intersects a positive cathode line. This will be further explained in conjunction with the specification. In any event, as one will ascertain, the display is formulated by a means of intersecting parallel lines which are insulated from each other. These lines form an XY matrix or an XY array and consist of grid lines and cathode lines arranged in a matrix. Hence, to access any particular point in a matrix, one must have an X and a Y address. The X and Y address is indicated by one grid line and one cathode line which intersect to form a pixel point or area and which point or area is written by causing pigment particles to migrate out of that pixel area on said display.

At the intersection of the X and Y addresses in the matrix, one will thereby provide a writing condition. In any event, as indicated above, when the grid potential becomes positive there is a decrease in the background brightness of the display due to the fact that the potential between the grid and cathode has changed for non-writing lines.

In addition, and of greater consequence, a dark line will appear at the leading edge of the picture being written (corresponding to the cathode at zero potential). The black line is indicative of the fact that all the pigment has left the cathode in the pixels being written. This is desirable, however, it is also noted that when the potential of the cathode

being written into is made positive, some of the pigment returns to the cathode resulting in incomplete writing and poor contrast. It is believed that this effect is probably due to the fact that the negatively charged pigment, which has only gone a short distance beyond the grid, is attracted back to the cathode by the combined positive grid and cathode fields. These factors substantially decrease the writing speed of such a display and provide a lack of contrast and so on, as described above.

It is the object of the present invention to apply selectable pulses to the grid and cathode electrodes during a write mode whereby the pulses supplied will serve to maintain the grid to cathode potential of non-writing electrodes at a fixed value which is indicative of a good contrast level. At the same time, a writing pulse applied to the grid remains for a given duration while the cathode to be written is held low for a longer duration. In this manner, one will have a positive grid potential at the start of writing a given pixel and a negative grid (which will repel the pigment that has traveled to the anode side of the grid) when writing of that pixel (cathode from zero to positive potential) is complete. In this manner, as will be explained, the effective speed of operation of the display is dramatically increased and results in a speed increase of approximately 6:1 over a conventional display operated according to the teachings of the prior art.

It is further indicated that the apparatus and method to be provided also pulses all cathodes which are not being written by a pulse of the same nature as the writing grid pulse. In this manner, the potential between the non-writing cathode lines and the grid lines remains constant and hence the above-noted problems are avoided.

Apparatus for driving an electrophoretic display in a write mode, which display is of the type having a plurality of grid lines insulated from a plurality of cathode lines with said grid and cathode lines positioned perpendicular to one another to provide an X-Y matrix. Said display having an anode electrode, said display enabling a picture to be displayed on said cathode by selectively accessing intersecting grid and cathode lines each indicative of a pixel and varying the bias between said lines to cause said particles to migrate to said anode for each selected intersection. The improvement in connection therewith comprising means coupled to said grid lines to provide a grid pulse on said lines, to be written of a given duration and of a given polarity and amplitude indicative of a write bias for said grid lines, means coupled to a selected intersecting cathode line associated with said grid line and selected according to a pixel to be written to provide a cathode pulse to said cathode line of an opposite polarity to said grid pulse and commencing at the start of said grid pulse but having a longer duration than said given duration whereby said cathode pulse is present when said grid pulse terminates. Apparatus for pulsing all non-writing cathodes with a pulse of the same amplitude and duration as the grid pulse.

FIG. 1 is a simple schematic view depicting an electrophoretic display according to this invention.

FIG. 2 is a schematic diagram showing an XY matrix array consisting of intersecting grid and cathode lines as provided in the electrophoretic display.

FIG. 3(A-C) is a series of timing diagrams showing the pulsing techniques according to this invention.

FIG. 4 is a schematic diagram showing a grid drive amplifying circuit employed in conjunction with this invention.

FIG. 5 is a schematic diagram showing a cathode drive amplifying circuit according to this invention.

Referring to FIG. 1 there is shown a simple schematic diagram necessary to indicate operation of a typical electrophoretic display. The reference numeral 11 refers to a cathode electrode which, as one will see from the above noted patents, is one of a number of a series of lines which are arranged, for example, in the horizontal or X direction. Each of these lines, as cathode lines, can be accessed or biased by means of a separate voltage applied to such a line. The associated grid lines are represented by reference numeral 12. Each grid structure, four of which are shown in FIG. 1, is insulated from the cathode lines by means of an insulator layer 13. The plate, or anode electrode, is referenced in FIG. 1 by reference numeral 15. In order to access a point on the matrix a potential is applied between the grid and cathode lines. This potential will access an intersection point in the X-Y matrix indicative of a pixel. In any event, the electrophoretic dispersion 16, which is located between the anode and cathode, contains a plurality of submicron pigment particles which can be charged according to known techniques.

The grid array, as indicated, overlies the cathode array and is insulated therefrom. When a given potential is applied between an X and Y point in the matrix, electrophoretic particles which are within the vicinity of the intersection between the grid and cathode structures are accelerated towards the anode. Particles, as 17 and 18, as indicated by the arrows, deposit on the plate or anode electrode and remain there until the charge or bias is reversed.

As one can ascertain from the above described prior art, the movement of the particles, as controlled by the intersection between an X and a Y line, causes these particles to migrate towards the anode. Thus, if the grid to cathode potential is

properly selected, electrophoretic particles which are negatively charged will be attracted towards the positive anode 15 which will assume the color of the pigment particles.

An image is formed on the cathode. The cathode image being a dark color, which is the color of the suspension medium in which the particles are suspended. As one can understand, the pigment particles are suspended in an electrophoretic dispersion and essentially are yellow particles in certain embodiments with the dispersion medium having a dark blue color. Thus, by viewing the cathode surface, either a yellow image on a dark blue background or a dark blue image on a yellow background may be viewed.

Referring to FIG. 2 there is shown a top view of a typical X-Y matrix consisting of cathode lines which are arranged in the horizontal plane and grid lines which are perpendicular to the cathode lines and which are insulated therefrom. Thus, referring to FIG. 2, there is shown four cathode lines designated as 20, 21, 22 and N. It is of course understood that the number of cathode lines in the Y direction may consist of hundreds or thousands, depending upon the size of the display.

As indicated, insulated from the cathode lines and perpendicular thereto, there are shown four grid lines 30, 31, 32 and X. It is also indicated that there can be many more grid lines associated with a typical display.

As seen in FIG. 2, each cathode line has a suitable driving amplifier circuit shown in modular form and indicated by reference numerals 40, 41, 42 and 43. In a similar manner, each grid line has a suitable driving amplifier referenced by modules 50, 51, 52 and 53. The driving signals for the grid and cathodes are obtained by typical driving generators as 60 and 61. As will be explained, these generators are such that they will provide the type of pulses necessary for the improved operation, as will be described in conjunction with the timing diagrams.

As indicated above, the display can typically be operated in an Erase Mode, a Hold Mode or a Writing Mode. In the Erase Mode the anode electrode, which is not shown in FIG. 2, is placed at a negative potential while the cathodes as lines 20-N are operated at a positive potential. In this mode the grid lines as 30 to X are operated at a low potential such a negative potential designated as zero for purposes of this discussion. In the hold mode the anode is positive while the cathodes are held positive and the grids are again at a low potential. As one can understand from the above, the cathode operates between zero and positive voltages. The grid operates between low and high voltages and for purposes of the present discussion a low will be indicative of zero and a high would be indicative of a 1.

In the Write Mode, the anode is held positive while cathode lines which are being written are placed at zero potential while non-writing cathodes are placed at positive potential. This is the same potential as employed in the Hold Mode. In this manner the writing grids are operated at a high potential and the non-writing grids are operated at the low potential or zero potential. This is exactly what the prior art taught in order to achieve the writing operation.

Based on prior art operation and looking at FIG. 2, the following problems occur. First let us assume that one desires to write at the intersection of cathode line 20 with grid line 30. In this manner grid line 30, via the driver amplifier 50, would be placed at the high or positive level. The cathode line 20, by means of the driver amplifier 40, would be set to a zero or ground potential. All other cathode lines, as 21, 23 and N would be set at a positive potential while all other non-writing grids, such as 31, 32 and X, would be set at the low potential. When the grid 30 has a positive potential applied thereto, an overwriting occurs between the intersections of grid 30 and cathode lines 21, 23 and N. As one can ascertain, the existence of the positive potential on the grid line 30 changes the cathode to grid voltage for lines 21, 23 and N. This causes an overwriting in each of these areas. This overwriting, essentially, reduces the effective contrast of the display.

In addition, and as indicated above, a dark line appears at the leading edge of the picture being written which corresponds to the cathode line 20 being at zero potential. Hence when the grid 30 is made positive a black line or an extremely black area appears at the intersection of cathode line 20 and grid line 30. This black line is indicative of the fact that all the pigment has left the cathode in the indicated area intersection between grid line 30 and cathode line 20. In any event, when the potential of the cathode line 20, which is being written, is made positive some of the pigment returns to the cathode area resulting in incomplete writing and poor contrast. As indicated above, this is probably due to the fact that the negatively charged pigment, which has only gone a short distance beyond the grid electrodes, is attracted back to the cathode by the combined positive grid and cathode fields. The amount returned is a function of writing speed.

Thus, as will be explained, in order to solve this problem it is indicated that the amplifiers as for example 50, 51, 52 and 53 will be operated so that there is a positive grid potential at the start of writing a given pixel and a negative grid potential which will repel the pigment that has traveled to the anode side of the grid when writing of that pixel as for example when the cathode goes from zero to

positive potential and therefore when the writing of that pixel is complete. Furthermore, the circuit will also operate to pulse all cathodes not being written in a positive potential direction and for a time duration exactly the same as the duration of the grid pulse. In this manner, all lines which are not being written maintain the same voltage difference between grid and cathode and hence do not degrade the brightness of the non-written areas. The cathode line that is being written is pulsed from a positive to a zero value for a duration longer than the duration of the grid pulse. In this manner the above-described problems have been substantially reduced.

For examples of typical timing diagrams, reference now will be made to FIG. 3. FIG. 3 shows the necessary timing relationships and waveforms for pulsing the grid and cathode electrodes according to the teachings of this invention. Referring to FIG. 3 there is shown three wave forms (A, B, C) indicative of the waveforms provided by the driving amplifiers and driving generators as 60 and 61 of FIG. 2 during the write mode. Let us assume, for example, that we are about to access the intersection between cathode line 20 and grid line 30. As shown in FIG. 3A, the grid line 30 will go from a given value, called $V_{dd}(V_G)$ to a positive value, thus exhibiting a positive peak of VP and for a duration of t seconds.

The waveform of FIG. 3B shows that cathode line 20 goes from V_{DD} (V_K) which is the hold voltage to zero or ground and remains for a duration of $t + \Delta t$ or for a longer duration than the pulse applied to the grid line 30. After the duration of $t + \Delta t$ cathode line 20 returns to the level V_{DD} - (V_k). At the same time the cathode lines as 21, 23 and N which are those lines that are not being written are pulsed with a transition from the V_{DD} voltage which is the Hold voltage in a positive direction to go to a level of $V_k + V_p$ where V_p is the same as V_p in FIG. 3A. The time duration of the cathode line pulse, time t, is the same as the duration of the grid pulse of FIG. 3A.

Thus, as explained, the above waveforms prevent the above-described problems whereby the cathode to grid potential of all cathode lines which are not being written into remains the same due to the pulsing of the non-writing cathode lines as shown in FIG. 3 as well as keeping the writing cathode at ground for a longer duration than the writing grid pulse.

Thus, the writing cathode line is held at zero potential for a longer duration than the positive pulse duration applied to the writing grid and non-writing cathodes therefore preventing the above-described problem whereby charged pigment will not be attracted back to the cathode by the combined positive grid and cathode fields as would be accomplished in the prior art. It is of course understood that one can write into multiple grid lines for each cathode line. In any event, if this occurs the same pulse configuration is generated by the circuitry for each of the grid lines to be written into in regard to the single cathode line as line 20 and the pulses having the time durations as depicted in the figure are appropriate.

In a typical display the following voltages were applicable. The voltage V_G was equal to -5 volts, the voltage V_k was equal to +19 volts, the voltage pulse V_p equals the +10 volts. The hold voltage, which is V_k-V_g was 24 volts while the grid transition went from -5 volts or from V_G to +5 volts indicative of a 10 volt peak (VP). The non-writing cathode transition is from V_k equal to +19 volts to $V_k + V_p$ equal to +29 volts. The duration of the grid pulse t is dependent upon the writing time for a particular line. Essentially one can write one line in 4 milliseconds whereby t would approximately equal 3 milliseconds with Δ t equal to 1 millisecond.

In a similar manner, if one had a maximum writing time say of 10 milliseconds or more, t would be equal to 7 or 8 milliseconds while Δ t would be 2 or 3 milliseconds or more. It is indicated that for writing times which exceed 10 milliseconds the duration of pulse t would stay at 7 or 8 milliseconds while the remaining time, Δ t, would vary accordingly.

Referring to FIG. 4 there is shown a typical grid driving amplifier such as employed for amplifiers 50, 51, 52 and 53. Essentially the amplifier has an input to driver 60 which is synchronous to the cathode scan and of a suitable width as described above in FIG. 3. It should be apparent to those skilled in the art that there are many techniques available for providing such pulses which are essentially as shown in FIG. 3.

The output of the driver 60 is coupled to a potentiometer 62 which is suitably biased and serves as the input to the operational amplifier 61 which also has a biasing adjustment coupled thereto. The potentiometers 62 and 63 are utilized to set the effective DC levels which are applied to the grid in regard to the pulse as shown for example in FIG. 3A.

In regard to FIG. 4 the driver stage 60 is implemented using an 7407 while the operational amplifier 61 is an MC4741. The driving amplifier is a DC amplifier to maintain the grid lines at a suitable level when writing does not occur.

Referring to FIG. 5 there is shown a schematic of the DC cathode amplifiers as for example amplifiers 40, 41, 42 and 43 of FIG. 2. Each cathode amplifier has a driver input stage 70 which receives an input the same as the input to driver 60 in FIG. 4. The output of the driver 70 is coupled via a potentiometer 71 to the input of an operational

amplifier 72 which also has its biasing adjusted by means of potentiometer 73. In this manner the output of the operational amplifier 72 is implemented to provide the pulse and DC levels as shown and necessary to drive the corresponding cathode lines as indicated in FIGS. 3B and C.

In regard to the schematic shown in FIG. 5, the inverter is also a 7404 integrated circuit while the operational amplifiers is an LM-2900. In view of the above, it should be apparent to those skilled in the art that the technique of driving the grid and cathode lines as described above enables faster display operation while circumventing many of the problems indicated above as associated with prior art displays and driving techniques.

Claims

1. An electrophoretic matrix display (Fig. 2) having:

a multiplicity of addressable intersections formed between a plurality of grid electrodes (30; 31; X) and a plurality of cathodes (20; 21; ....; N);

grid address means (60, 50, 51, ..., 53) coupled to the plurality of grid electrodes (30, 31, ..., X) and arranged to apply a grid pulse (A) to a selected one (30) thereof; and,

cathode address means (61, 40, 41, ..., 43) coupled to the plurality of cathodes (20, 21, ..., N) and arranged to apply a cathode pulse (B) to a selected one (20) thereof thereby to establish a write bias at an addressed intersection formed between the selected grid electrode (30) and the selected cathode (20);

characterised in that

the cathode address means (61, 40, 41, ..., 43) is adapted to apply the cathode pulse (B) for a duration ($t+\Delta t$) that is larger than that (t) for the grid pulse (A) and such that it (B) shall persist (Δt) following termination of the grid pulse (A).

2. A display, as claimed in claim 1, wherein the grid address means (60, 50, 51,..., 53) is arranged to apply the grid pulse (A) for a duration (t) of between 3 and 8 milliseconds; and

the cathode address means (61, 40, 41,..., 43) is adapted to apply the cathode pulse (B) for a duration ($t+\Delta t$) of between 4 and 20 milliseconds.

3. A display, as claimed in either preceding claim 1 or claim 2,

further characterised in that:

the cathode address means (61, 40, 41, ..., 43) is adapted to apply an additional cathode pulse (C) to each remaining cathode (21, 23, ... N) thereby to reduce any change in a predetermined bias between each remaining cathode (21, 23, ..., N) and the selected grid electrode (30) when the grid pulse (A) is applied.

4. A display, as claimed in claim 3, wherein:

the grid address means (60, 50, 51, ..., 53) and the cathode address means (61, 40, 41, ..., 43) are adapted to co-operate such that the grid pulse (A) and each additional cathode pulse (C) are coincident, and of the same polarity sense and magnitude (Vp) so that the predetermined bias between the selected grid electrode (30) and each remaining cathode (21, 23, ..., N) shall in each case be maintained constant when the grid pulse (A) is applied.

5. A method of operating an electrophoretic matrix display wherein:

a grid pulse is applied to a selected grid electrode; and

a cathode pulse is applied to a selected cathode to establish a write bias at an addressed intersection formed between the selected grid electrode and the selected cathode;

characterised in that

the cathode pulse is applied for a longer duration than the grid pulse so that the selected cathode is maintained at a pulse level after the grid pulse has terminated.

6. A method, as claimed in claim 5, wherein:

the grid pulse is applied for a duration of between 3 and 8 milliseconds; and

the cathode pulse is applied for a duration of between 4 and 20 milliseconds.

7. A method, as claimed in either preceding claim 5 or claim 6,

further characterised in that:

an additional cathode pulse is applied to each remaining cathode intersecting the selected grid electrode, which pulse is in each case coincident with the grid pulse and is such as to reduce any change in predetermined bias between the selected grid electrode and the remaining cathode to which it is applied when the grid pulse is applied to the selected grid electrode.

8. A method, as claimed in claim 7, wherein:

the additional cathode pulse is in each case of the same polarity sense and amplitude as the grid pulse such that the predetermined bias between the selected grid electrode and the remaining cathode to which it is applied is maintained constant when the grid pulse is applied.

Patentansprüche

1. Elektrophoretische Matrixanzeige (Fig. 2) mit:

einer Mehrzahl zwischen einer Anzahl Rasterelektroden (30; 31; X) und einer Anzahl Kathoden (20; 21; ....; N) gebildeter adressierbarer Kreuzungspunkte;

einer mit der Anzahl Rasterelektroden (30, 31, ..., X) gekoppelten und zum Aufbringen eines Rasterimpulses (A) auf eine ausgewählte (30) Rasterelektrode eingerichteten Raster-Adresseinrichtung (60, 50, 51, ..., 53), und

einer mit der Anzahl Kathoden (20, 21, ..., N) gekoppelten und zum Aufbringen eines Kathodenimpulses (B) auf eine ausgewählte (20) Kathode eingerichteten Kathoden-Adresseinrichtung (61, 40, 41, ..., 43), wobei dadurch eine Schreib-Vorspannung bei einem zwischen der ausgewählten Rasterelektrode (30) und der ausgewählten Kathode (20) gebildeten adressierbaren Kreuzungspunkt hergestellt wird;

dadurch gekennzeichnet, daß

die Kathoden-Adresseinrichtung (61, 40, 41, ..., 43) zum Aufbringen des Kathodenimpulses (B) während einer Dauer (t + Δt) eingerichtet ist, die länger ist als diejenige (t) für den Rasterimpuls (A) und derart, daß der Kathodenimpuls (B) nach der Beendigung des Rasterimpulses (A) anhält (Δt).

2. Anzeige nach Anspruch 1, wobei die Raster-Adresseinrichtung (60, 50, 51, ..., 53) zum Aufbringen des Rasterimpulses (A) für eine Dauer (t) zwischen 3 und 8 Millisekunden eingerichtet ist und die Kathoden-Adresseinrichtung (61, 40, 41,..., 43) zum Aufbringen des Kathodenimpulses (B) für eine Dauer (t + Δt) zwischen 4 und 20 Millisekunden eingerichtet ist.

3. Anzeige nach einem der vorstehenden Ansprüche 1 oder 2, ferner dadurch gekennzeichnet, daß die Kathoden-Adresseinrichtung (61, 40, 41, ..., 43) zum Aufbringen eines zusätzlichen Kathodenimpulses (C) auf jede verbleibende Kathode (21, 23, ..., N) eingerichtet ist, um dadurch jegliche Veränderung einer vorbestimmten Vorspannung zwischen jeder verbleibenden Kathode (21, 23, ..., N) und der ausgewählten Rasterelektrode (30) zu vermindern, wenn der Rasterimpuls (A) aufgebracht wird.

4. Anzeige nach Anspruch 3, wobei die Raster-Adresseinrichtung (60, 50, 51, ..., 53) und die Kathoden-Adresseinrichtung (61, 40, 41, ..., 43) derart zur Zusammenarbeit eingerichtet sind, daß der Rasterimpuls (A) und jeder zusätzliche Kathodenimpuls (C) gleichzeitig auftreten und von gleicher Polarität und Größe (Vp) sind, so daß die vorbestimmte Vorspannung zwischen der ausgewählten Rasterelektrode (30) und jeder verbleibenden Kathode (21, 23, ..., N) auf jeden Fall konstant gehalten wird, wenn der Rasterimpuls (A) angelegt ist.

5. Verfahren zum Betreiben einer elektrophoretischen Matrixanzeige, wobei

ein Rasterimpuls an eine ausgewählte Rasterelektrode angelegt wird; und

ein Kathodenimpuls an eine ausgewählte Kathode angelegt wird, um eine Schreib-Vorspannung bei einem zwischen der ausgewählten Rasterelektrode und der ausgewählten Kathode gebildeten adressierbaren Kreuzungspunkt herzustellen;

dadurch gekennzeichnet daß,

der Kathodenimpuls für eine längere Dauer als der Rasterimpuls angelegt wird, so daß die ausgewählte Kathode auf einem Impuls-Pegel gehalten wird, nachdem der Rasterimpuls beendet ist.

6. Verfahren nach Anspruch 5, wobei der Rasterimpuls während einer Dauer von zwischen 3 und 8 Millisekunden angelegt wird und der Kathodenimpuls während einer Dauer von zwischen 4 und 20 Millisekunden angelegt wird.

7. Verfahren nach einem der vorstehenden Patentansprüche 5 oder 6, ferner dadurch gekennzeichnet, daß ein zusätzlicher Kathodenimpuls an jede die ausgewählte Rasterelektrode kreuzende verbleibende Kathode angelegt wird, wobei der Impuls auf jeden Fall gleichzeitig mit dein Rasterimpuls derart auftritt, daß jede Änderung der vorbestimmten Vorspannung zwischen der ausgewählten Rasterelektrode und der verbleibenden Kathode, an welche dieser angelegt wird, wenn der Rasterimpuls an die ausgewählte Rasterelektrode angelegt ist, vermindert wird.

8. Verfahren nach Anspruch 7, wobei der zusätzliche Kathodenimpuls auf jeden Fall von gleicher Polarität und Amplitude wie der Rasterimpuls ist, so daß die vorbestimmte Vorspannung zwischen der ausgewählten Rasterelektrode und der verbleibenden Kathode, an die dieser angelegt ist, konstant gehalten wird, wenn der Rasterimpuls angelegt ist.

Revendications

1. Afficheur à matrice électrophorétique (Figure 2) comportant :

une multiplicité d'intersections adressables formées entre une pluralité d'électrodes de

grilles (30 ; 31 ; X) et une pluralité de cathodes (20 ; 21 ; ... ; N) ;

un moyen d'adresse de grille (60, 50, 51, ..., 53) couplé à une pluralité d'électrodes de grilles (30; 31, ..., X) et agencé pour appliquer une impulsion de grille (A) à une grille sélectionnée (30) parmi ces grilles ; et

un moyen d'adresse de cathode (61, 40, 41, ..., 43) couplé à une pluralité de cathodes (20, 21, ..., N) et agencé pour appliquer une impulsion de cathode (B) à une cathode sélectionnée parmi ces cathodes, établissant ainsi une polarisation d'écriture à une intersection adressée formée entre l'électrode de grille sélectionnée (30) et la cathode sélectionnée (20) ;

caractérisé en ce que

le moyen d'adresse de cathode (61, 40, 41, ..., 43) est adapté pour appliquer l'impulsion de cathode (B) pendant une durée de temps égale à (t + Δt) qui est supérieure à la durée (t) correspondant à l'impulsion de grille (A) et de manière à ce que l'impulsion (B) persiste pendant un temps (Δt) qui suit la terminaison de l'impulsion de grille (A).

2. Afficheur selon la revendication 1, dans lequel

le moyen d'adresse de grille (60, 50, 51, ..., 53) est agencé pour appliquer une impulsion de grille (A) pendant une durée (t) comprise entre 3 et 8 millisecondes ; et

un moyen d'adresse de cathode (61, 40, 41, ..., 43) adapté pour appliquer une impulsion de cathode (B) pendant une durée de temps égale à (t + Δt) comprise entre 4 et 20 millisecondes.

3. Afficheur selon l'une quelconque des revendications 1 ou 2,

caractérisé en outre en ce que :

le moyen d'adresse de cathode (61, 40, 41, ..., 43) est adapté pour appliquer une impulsion de cathode supplémentaire (C) à chacune des cathodes restantes (21, 23, ..., N) afin de réduire ainsi toute variation de la polarisation prédéterminée existant entre chaque cathode restante (21, 23, ..., N) et l'électrode de grille sélectionnée (30) lorsque l'impulsion de grille (A) est appliquée.

4. Afficheur selon la revendication 3, dans lequel :

le moyen d'adresse de grille (60, 50, 51, ..., 53) et le moyen d'adresse de cathode (61, 40, 41, ..., 43) sont adaptés pour coopérer de telle sorte que l'impulsion de grille (A) et chaque impulsion de cathode supplémentaire (C) coïncident et aient le même sens de polarité et la même grandeur (V_p) de telle sorte que la polarisation prédéterminée entre l'électrode de grille sélectionnée (30) et chacune des cathodes restantes (21, 23, ..., N) soit dans chaque cas maintenue constante lorsque l'impulsion de grille (A) est appliquée.

5. Procédé pour le fonctionnement d'un afficheur à matrice électrophorétique, dans lequel :

une impulsion de grille est appliquée à une électrode de grille sélectionnée ; et

une impulsion de cathode est appliquée à une cathode sélectionnée pour établir une polarisation d'écriture sur une intersection adressée formée entre l'électrode de grille sélectionnée et la cathode sélectionnée ;

caractérisé en ce que

l'impulsion de cathode est appliquée pendant une durée plus longue que l'impulsion de grille de telle sorte que la cathode sélectionnée est maintenue a un niveau d'impulsion après la terminaison de l'impulsion de grille.

6. Procédé selon la revendication 5, dans lequel :

l'impulsion de grille est appliquée pendant une durée comprise entre 3 et 8 millisecondes ; et

l'impulsion de cathode est appliquée pendant une durée comprise entre 4 et 20 millisecondes.

7. Procédé selon l'une quelconque des revendications 5 ou 6,

caractérisé en outre en ce que :

une impulsion de cathode supplémentaire est appliquée à chacune des cathodes restantes qui est en intersection avec une électrode de grille sélectionnée, ladite impulsion est dans chaque cas en coïncidence avec l'impulsion de grille et est telle qu'elle réduit toute variation de la polarisation prédéterminée entre l'électrode de grille sélectionnée et la cathode restante à laquelle elle est appliquée lorsque l'impulsion de grille est appliquée à l'électrode de grille sélectionnée.

8. Procédé selon la revendication 7, dans lequel :

l'impulsion de cathode supplémentaire a dans chaque cas le même sens de polarité et la même amplitude que l'impulsion de grille, de telle sorte que la polarisation prédéterminée entre l'électrode de grille sélectionnée et la cathode restante à laquelle elle est appliquée est maintenue constante lorsque l'impulsion de grille est appliquée.

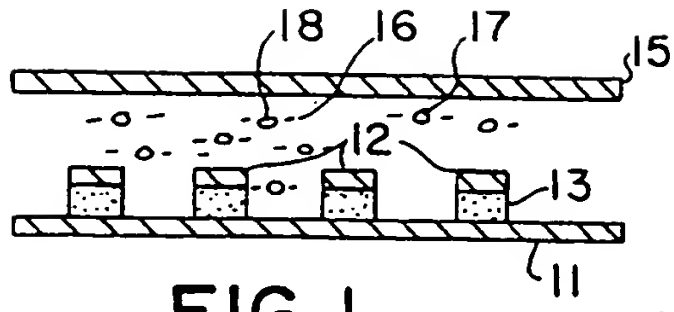
18
16
17
15
12
13
11

FIG. 1

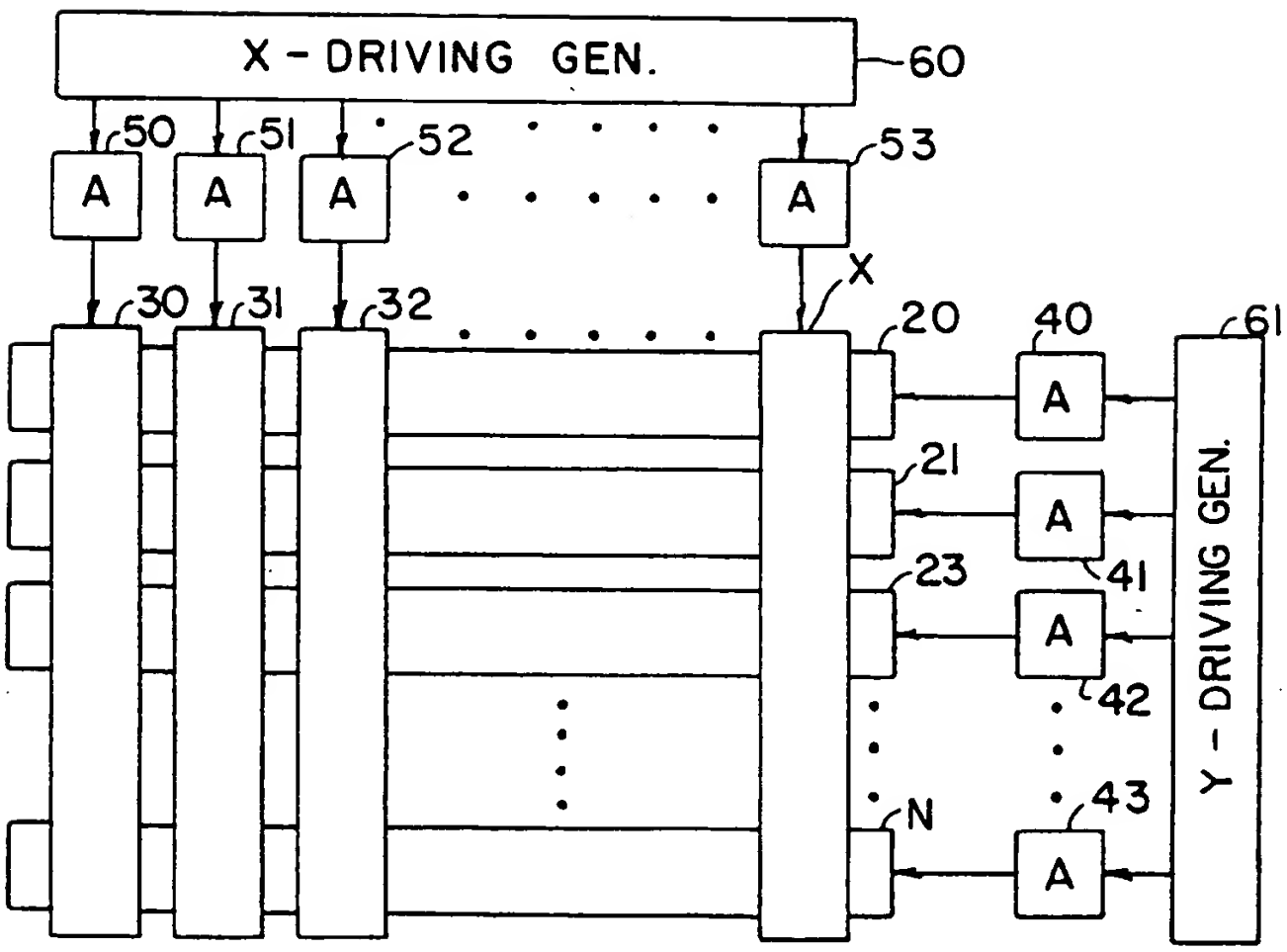
X - DRIVING GEN.
60
50
51
52
53
A
30
31
32
X
20
40
61
21
23
41
42
43
N
Y - DRIVING GEN.

FIG. 2

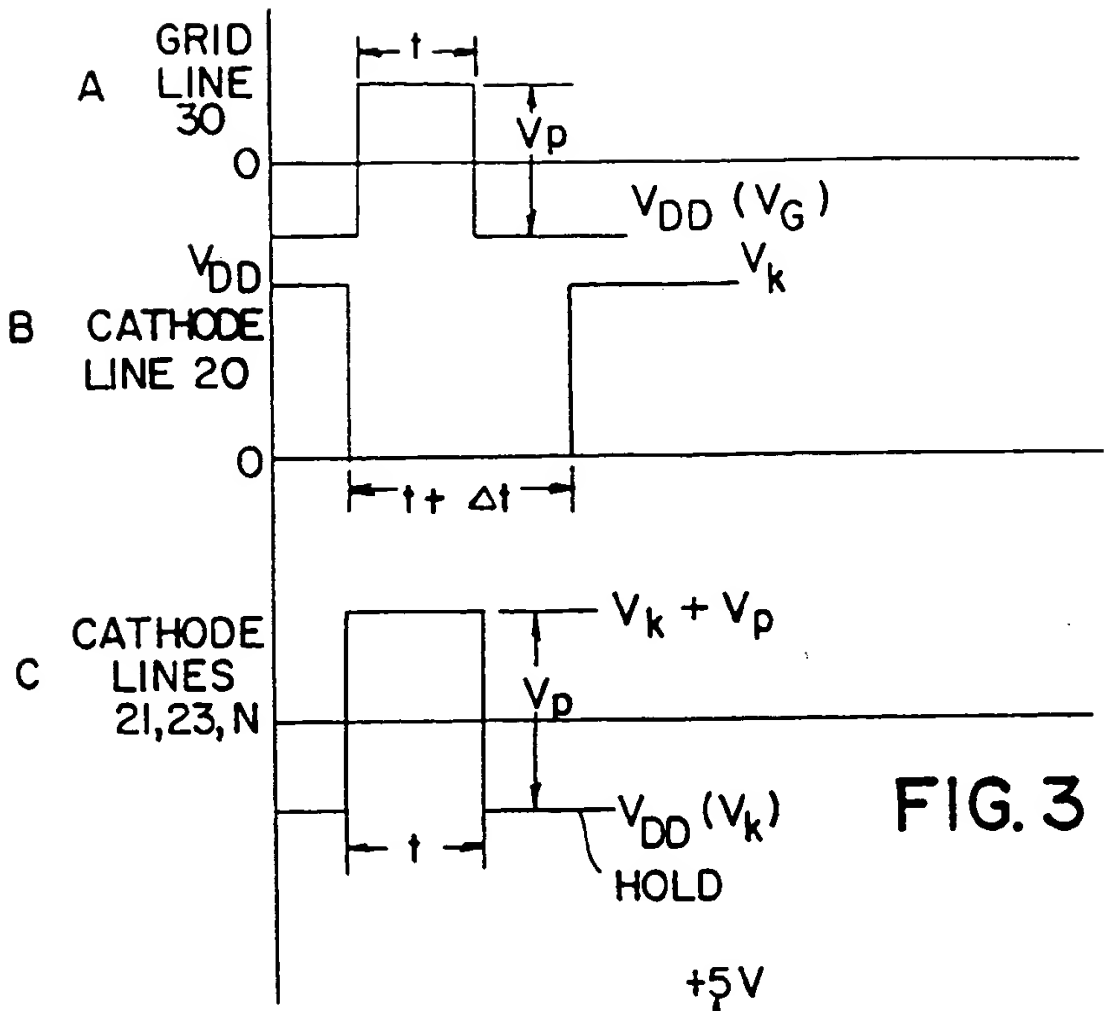

FIG. 3

FIG. 4

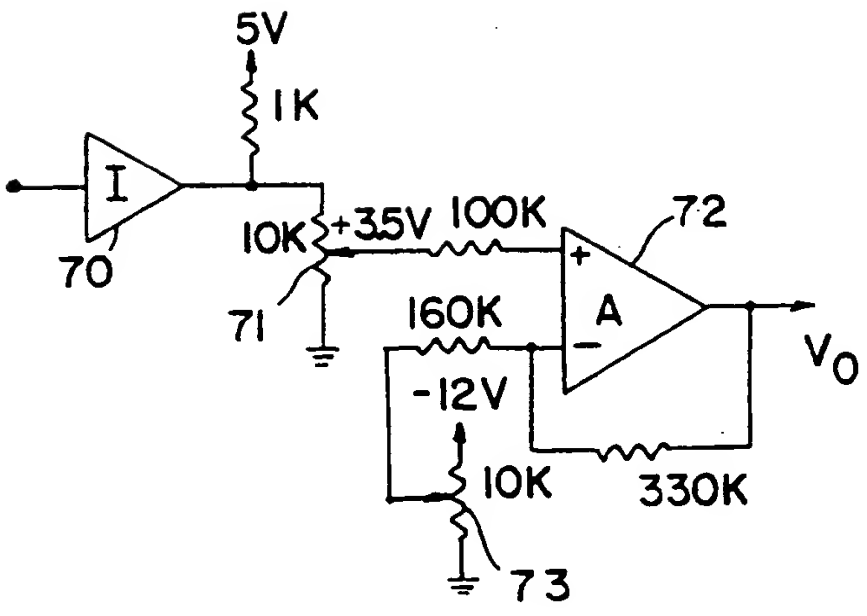

FIG. 5

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 390 303 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90250085.9

(51) Int. Cl.5: G06F 15/02

(22) Date of filing: 30.03.90

The title of the invention has been amended (Guidelines for Examination in the EPO, A-III, 7.3).

(30) Priority: 31.03.89 JP 78465/89
15.05.89 JP 120651/89
15.05.89 JP 120652/89
07.06.89 JP 143146/89
26.07.89 JP 191399/89
05.10.89 JP 258888/89

(43) Date of publication of application:
03.10.90 Bulletin 90/40

(84) Designated Contracting States:
DE FR GB

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(54) Electronic notebook.

(57) An electronic system pocketbook apparatus includes a foldable and portable main body, an expansion card holder mounted on the main body, a necessary number of expansion cards held by the expansion card holder, and a communicating unit. The main body has functions of right and left portions coupled by a cover, is folded upon carrying of the main body so that the right portion overlaps the left portion, a folded portion being fastened by a cover clip provided to the cover, and has basic functions of controlling arithmetic operations and display data processing by using an internal controller, data inputting means, and displaying data on a display unit. The communicating unit performs data transmission/reception between the held expansion cards and the main body via the expansion card holder.

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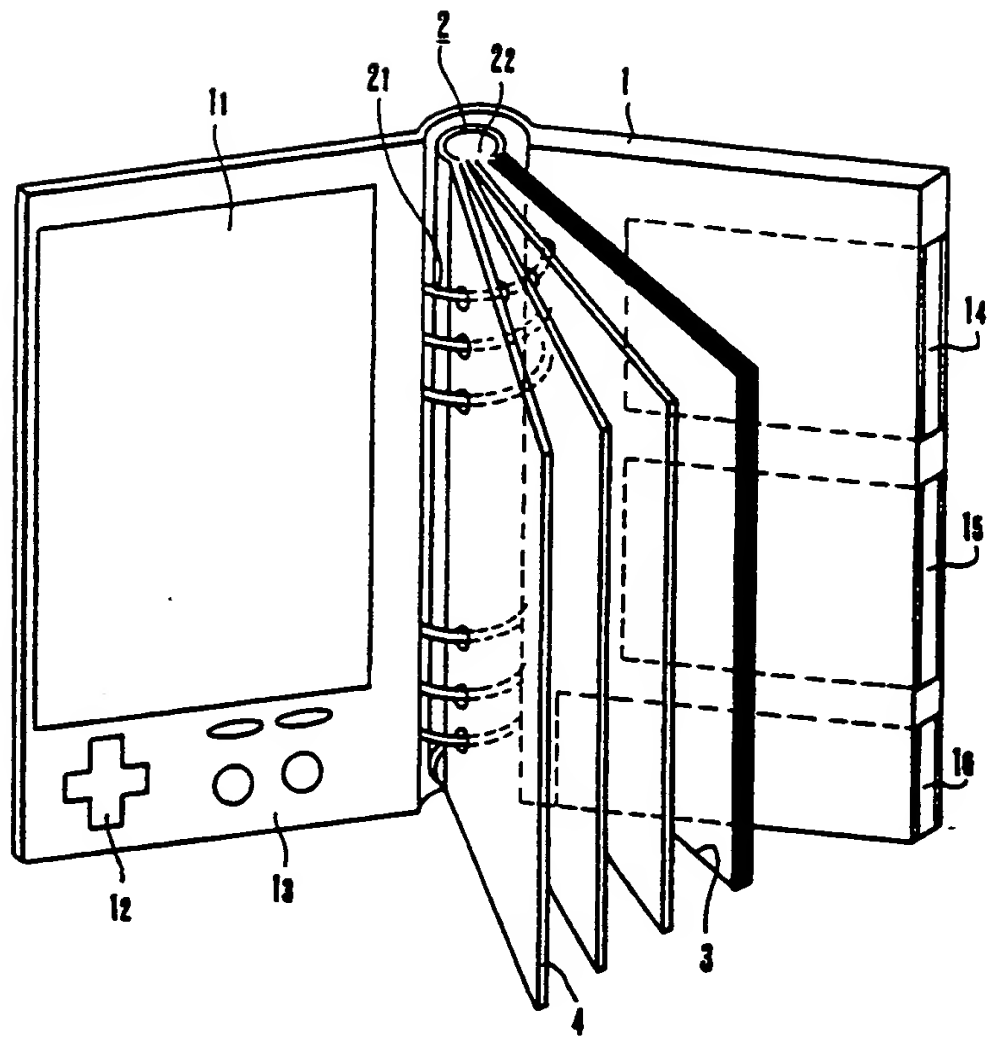


FIG.1

Electronic System Pocketbook Apparatus

Background of the Invention

The present invention relates to an electronic system pocketbook apparatus having an electronic processing function.

Conventionally, system pocketbooks have been widely used by office workers for schedule adjustment, memos, and the like. A system pocketbook has a recording paper holder for holding recording paper, and a user writes necessary contents on recording paper held by the recording paper holder. A system pocketbook apparatus of this type, however, is inconvenient since the recording paper must be replaced each year. In order to eliminate this inconvenience, some devices are disclosed in Published Unexamined Patent Application Nos. 62-107360, 59-68072, and the like. In each of these disclosed devices, a memory card stores necessary contents.

These advanced devices, however, are still unsatisfactory since in order to process a plurality of types of data, a memory card of the apparatus must be replaced for each type of data.

Summary of the Invention

It is, therefore, a principal object of the present invention to provide an electronic system pocketbook apparatus capable of attaching/detaching a plurality of data bases and arbitrarily determining the number of data bases to be used.

It is another object of the present invention to provide an electronic system pocketbook apparatus smaller than a conventional apparatus.

It is still another object of the present invention to provide an electronic system pocketbook apparatus capable of holding basic constituting elements required as an electronic pocketbook as many as possible in a limited space.

In order to achieve the above objects of the present invention, there is provided an electronic system pocketbook apparatus comprising a foldable and portable main body having functions of right and left portions coupled by a cover, folded upon carrying of the main body so that the right portion overlaps the left portion, a folded portion being fastened by a cover clip provided to the cover, and having basic functions of controlling arithmetic operations and display data processing by using an internal controller, data inputting means, and displaying data on a display unit, an expansion card holder mounted on the main body, a necessary number of expansion cards held by the expansion card holder, and communicating means for performing data transmission/reception between the held expansion cards and the main body via the expansion card holder.

Brief Description of the Drawings

Fig. 1 is a perspective view showing an embodiment of the present invention;

Figs. 2(a) to 2(h) are views each showing an information input means;

Fig. 3 is a view showing a method of housing an information input means;

Fig. 4 is a view showing an inserting/removing structure of an LCD;

Figs. 5(a), 5(b), and 5(c) are views showing a structure for illuminating the LCD;

Figs. 6 to 11 are views each showing a communicating means between a main body and an expansion card;

Figs. 12(a), 12(b), and 13 are views each showing a state in which the direction of a cursor pad is physically changed;

Figs. 14(a) and 14(b) are block diagrams showing a circuit for stopping supply of power when an expansion card holder is opened;

Fig. 15 is a flow chart for explaining an operation of the circuit shown in Figs. 14(a) and 14(b);

Fig. 16 is a perspective view showing a state in which a cover clip is closed;

Fig. 17 is a sectional view showing a structure for using the cover clip as a switch;

Fig. 18 is a circuit diagram showing a circuit for controlling a clock oscillator by an ON/OFF operation of the cover clip;

Figs. 19(a) to 19(j) are timing charts for explaining an operation of the circuit shown in Fig. 18;

Figs. 20 and 21 are flow charts for explaining operations of the circuit shown in Fig. 18;

Fig. 22 is a circuit diagram showing a circuit used to directly switch on/off a power source by a cover switch;

Fig. 23 is a circuit diagram showing a circuit used to indirectly switch on/off the power source by the cover switch;

Figs. 24(a), 24(b), 25(a), and 25(b) are a perspective view and sectional views, respectively, each showing a structure for using the cover clip as a switch;

Fig. 26 is a perspective view showing a structure for housing batteries in a lower space of the expansion card holder;

Fig. 27 is a perspective view showing a battery holder;

Fig. 28 is a perspective view of a battery;

Fig. 29 is a perspective view of the expansion card holder;

Fig. 30 is a view showing a state in which a screen is divided into a plurality of blocks;

Fig. 31 is a block diagram showing a circuit used to output a touched key code;

Fig. 32 is a view showing another communication method between the expansion card and the main body;

Figs. 33(a) and 33(b) are views each showing a modification of the expansion card structure for performing the communication method shown in Fig. 32;

Fig. 34 is a perspective view showing a structure of a display;

Fig. 35 is a block diagram showing a circuit for connecting a moving direction of a cursor when a longitudinal/lateral direction of the display is changed;

Fig. 36 is a view for explaining a structure for detecting the longitudinal/lateral direction of the display in accordance with a holding direction;

Fig. 37 is a flow chart for explaining an operation for correcting the moving direction of the cursor when the longitudinal/lateral direction of the display is changed;

Figs. 38 and 39 are perspective views showing an electromagnetic coupling means arranged at the expansion card holder side to perform communication between the expansion card holder and the expansion card;

Fig. 40 is a view showing an electromagnetic coupling means arranged at the expansion card side;

Fig. 41 is a circuit diagram showing a circuit for performing electromagnetic-coupled communication between the expansion card holder and the expansion card;

Fig. 42 is a view showing a signal format for performing communication between the expansion card holder and the expansion card; and

Figs. 43(a) to 43(e) are views showing signal waveforms for explaining a signal waveform change upon transmission of one bit of data.

Detailed Description of the Preferred Embodiment

Fig. 1 shows an electronic system pocketbook apparatus according to an embodiment of the present invention. Referring to Fig. 1, reference numeral 1 denotes a portable electronic system pocketbook main body having a foldable structure; 1_1, a display unit; 1_2, a cursor key; 1_3, a function key; 1_4 and 1_5, IC cards; and 1_6, a power source. The main body 1 has an internal CPU (not shown) and processing function units for performing necessary data processing at its both sides.

An expansion card holder 2 is constituted by rings 2_1 for holding an expansion card 4 and/or recording paper 3 and an opening/closing metal piece 2_2 for opening/closing the rings 2_1. That is, the expansion card holder 2 also holds the recording paper 3. Transmission/reception of necessary data between the expansion card 4 and the main body 1 is performed by a communicating means (to be described later).

In the apparatus having the above arrangement, data is normally input by an input means such as keys provided on the expansion card 4. If, however, data must be input by handwriting, a user can write necessary characters with a pen on the display unit 1_1 to perform handwriting input. For this purpose, as shown in Fig. 2(a), the display unit 1_1 has a pressure sensor 5 on which a user can write necessary characters or graphic patterns with a pen 6. The pen 6 consists of a hard material such as plastic and is formed to have a thin distal end and a thick rear end as shown in Fig. 2(c). When the thin portion of the pen 6 is used to write necessary information on a screen as shown in Fig. 2(a), an output is generated from only a narrow portion of the pressure sensor as indicated by a symbol ℓ_1 in Fig. 2(a). When the thick portion of the pen 6 is used to input necessary information as shown in Fig. 2(b), an output is generated from a wide portion as indicated by symbol ℓ_2 in Fig. 2(b). Therefore, by programming the apparatus such that

information is written when an output is generated from a narrow portion and written information is erased when an output is generated from a wide portion, switching between information writing and erasing functions can be performed without a troublesome operation of, e.g., manipulating a switch. The pen 6 may have two ends having the same thickness as shown in Fig. 2(d). In this case, a soft member 6_1 such as rubber, for example, is attached to the rear end of the pen 6. When the screen is pressed by a hard portion of the pen 6, an output signal is generated from a narrow range. When the screen is pressed by the soft portion 6_1, however, an output signal is generated from a wide range since the soft portion is distorted. As a result, information writing and erasing operations can be distinguished from each other as described above. With this arrangement, a user can write and erase information as if he or she were using a normal eraser. The pen 6 is preferably housed in an upper portion of the display unit 1_1 as shown in Fig. 3 for the sake of convenience in use. The distal end shape of the pen may be changed as shown in Figs. 2(e) to 2(g). When the screen is pressed by the pen, the distal end shape of the pen is detected to determine a processing command. In addition, as shown in Fig. 2(h), the pen may be modified such that its sharp distal end is used to perform writing and erasing and its side wall s of a flat shape is used to perform switching between writing and erasing modes. This switching may be realized by using a switch.

The display unit 1_1 can display a plurality of keys on its display screen and detect a coordinate point of a touched portion to determine that a key corresponding to the portion is manipulated. In this case, the surface of the display unit 1_1 may comprise a pressure sensor as shown in Figs. 2(a) and 2(b) or a touch panel as shown in Fig. 4. Fig. 4 shows a structure in which a touch panel 7 is used as the display unit 1_1 and a liquid crystal display (to be referred to as an LCD hereinafter) 8 can be inserted in/removed from the touch panel 7. In this manner, a user can use an economical LCD at the beginning and later on replace the economical LCD with an LCD which is expensive but has high resolution, if necessary. Referring to Fig. 4, reference numeral 15 denotes a lever for unlocking a mechanical lock in order to remove the LCD 8. Although a display using an LCD can be seen in a bright place, it is difficult to see the display in a dark place. In this case, as shown in Fig. 5(a), a light-emitting member such as an EL 9 is placed below the LCD 8 so that display visibility is improved by light emitted by the EL 9. The EL 9 receives a voltage via an electrode 12 in contact with an electrode 11 at the display side and emits light. Since, however, a considerable amount of power is consumed upon light emission, a reflecting plate 10 may be adhered on the rear side of the EL 9 so that the member (an auxiliary display 13 obtained by adhering the EL 9 and the reflecting plate 10) can be turned over when light emission is not necessary. Fig. 5(b) shows the auxiliary display 13 in detail, and Fig. 5(c) shows the LCD 8 in detail. Referring to Fig. 5(c), power is supplied from an electrode 14 at the main body side via an electrode 8_1 of the LCD. Note that a recess portion 8_2 is formed in the LCD 8 to receive the reflecting plate 10 when the auxiliary display 13 is turned over.

In order to use an expansion card, signal exchange must be performed between the card and the main body. Fig. 6 shows a communication means for performing this signal exchange. Referring to Fig. 6, an optical connector 18_1 provided at the distal end of an optical fiber cable 18 connected to the expansion card 4 is fitted in a connector 18_2 at the main body side. Although only one optical fiber cable is shown in Fig. 6, two cables may be used to perform full-duplex communication. Fig. 7 shows another communication means in which cores 19_1 and 19_2 are provided to the expansion card 4 so as to be perpendicular to the rings 2_1 for holding the expansion card and cores 19_3 and 19_4 are provided at the main body side. With this arrangement, communication can be performed by an electromagnetic induction effect obtained via the rings 21 without using any special connection. Fig. 8 shows a means in which light-emitting diodes 20_1 and 21_2 are provided at the expansion card 4 side and light-receiving diodes 20_2 and 21_1 are provided at the main body side, thereby performing signal transmission by optical communication between the light-emitting and light-receiving diodes. In this arrangement, although the optical axes of the light-emitting and light-receiving diodes do not oppose each other, communication can be performed by scattered light since the distance is short. Since, however, a transmission efficiency of this means is not so high, a means shown in Fig. 9 is more advantageous in order to increase the efficiency. Referring to Fig. 9, light emitted from a light-emitting diode is reflected by a ring 2_1 and the reflected light is guided to a light-receiving diode 21_1. In addition, as illustrated by a sectional view of a ring shown in Fig. 10, the transmission efficiency can be further increased by forming a recess-like groove 22 in the inner surface of the ring 2_1 so as to efficiently reflect light. Fig. 11 shows a method using electromagnetic induction. In the method shown in Fig. 11, not a magnetic flux but a current is flowed to the ring 2_1, and a coil 23 is provided at the expansion card 4 side, thereby coupling the coil and ring by electromagnetic induction.

Figs. 12(a) and 12(b) are views for explaining a method of mechanically rotating the cursor key pad 1_2 to cope with a display direction change. In this method, the cursor key pad located at a position shown in Fig. 12(a) is moved along a cursor moving direction as shown in Fig. 12(b). With this arrangement, since the upper portion of the cursor key always points the upper portion of the screen, a user does not feel

inconvenience upon operation. Fig. 13 shows another method of rotating the cursor key pad, in which projections 30_1 to 30_4 (30_4 is not shown in Fig. 13) are engaged with grooves 31_1 and 31_2 to rotate the cursor key pad.

Figs. 14(a) and 14(b) show a side view of the expansion card holder 2 (the expansion card holder shown in Fig. 1 viewed from the above) associated with the arrangement shown in Fig. 11 for performing communication between the main body and the expansion card. Fig. 14(a) shows the ring 2_1 in a closed state, and Fig. 14(b) shows the ring 2_1 in a closing released state, i.e., in an open state. The ring 2_1 is mounted on a mounting plate 2_8. When the ring 2_1 is closed, a projection 2_4 of a switch 2_3 is urged against the mounting plate 2_8 to turn on the switch 2_3 as shown in Fig. 14(a). When the ring 2_1 is opened as shown in Fig. 14(b), urging of the projection 2_4 is released to turn off the switch 2_3.

The expansion card 4 receives a current for communication from a constant current source 2_5 provided at the main body side via the ring 2_1. Therefore, when the ring 2_1 is opened as shown in Fig. 14(b), a voltage at the open end of the ring may rise to give a shock to a finger or the like of a user. Therefore, a controller 2_6 detects the open state of the ring 2_1 in accordance with the state of the switch 2_3 to stop the operation of the constant current source 2_5.

Since communication is performed between the main body and the expansion card via the ring 2_1, communication for the expansion card performed via the ring 2_1 is interrupted when the ring 2_1 is opened. If this state is kept unchanged, a timing difference is produced between processing performed at the main body side and processing performed at the expansion card. In order to prevent such an inconvenience, according to the present invention, when the switch 2_3 is turned off, both of a processor 2_7 at the main body side and a processor at the expansion card side stop their operations.

In this manner, after the ring 2_1 is opened, data processing operations at both the main body and expansion card sides are stopped, and communication between the main body and the expansion card is also stopped. If, however, the ring 2_1 is closed, communication is restarted, and the stopped data processing is also restarted.

Since, however, the expansion card cannot directly use an open/close signal from the switch 2_3, control is performed by a method as shown in Fig. 15.

That is, when the state of the switch 2_3 changes, a signal indicating the change is transmitted to the CPU at the main body side to set the CPU in an interruption state. If the CPU determines in step 200 that the switch 2_3 is turned off by this interruption, the CPU generates a sleep command for stopping the operation at the expansion card side as shown in step 201. As a result, the command is transmitted to the expansion card 4 to set the expansion card 4 in a sleep state, thereby stopping communication and the data processing. Meanwhile, in order to prepare for an operation to be performed when the power source is switched on next, the main body side stores states of the respective sections and starts a sleep state in step 202, thereby stopping communication and the operation. In this manner, a power consumption can be largely reduced by setting the sleep state. Note that the sleep state is an operation in which a clock signal is stopped to stop the operation of the CPU.

When the ring 2_1 is closed and a clock signal is generated accordingly, an operation is restarted from the start timing in the interruption state shown in Fig. 15. The CPU determines an ON state of the switch 2_3 in step 200A and transmits a sleep release command to the expansion card side in step 204A. As a result, the operation from the timing at which the operation is stopped is restarted to perform a normal operation (step 205A).

When the ring 2_1 is opened while the expansion card receives power supply from the main body, the expansion card stops its operation (step 201A) since the power is no longer supplied to the expansion card. In this state, however, the main body continues its operation since power is supplied to circuits at the main body side. Therefore, if this state is kept unchanged, a timing difference is produced between processing at the main body side and that at the expansion card side. In order to prevent such an inconvenience, according to the present invention, when the switch 2_3 is turned off, the operation of the processor 2_7 at the main body side is stopped on the basis of a signal indicating the OFF state of the switch 2_3 (step 202A). As a result, data processing is stopped from the timing at which the ring 2_1 is opened, and communication between the main body and the expansion card is also stopped.

When the ring 2_1 is closed, however, power is supplied to the expansion card, and the stopped data processing is restarted (step 204A).

Fig. 16 shows an apparatus in which a power source operates when a cover is opened. Referring to Fig. 16, reference numeral 201 denotes a data processor; 202, a cover of a pocket book; and 203, a cover clip for closing the cover 202 when the pocketbook is not used. The cover clip 203 can be fastened by a cover fastening button 204. As shown in Fig. 17, for example, an engaging portion 204_1 is formed inside the cover fastening button 204 and engaged with a projecting portion 202_1 formed at the cover 202 side, thereby

fastening the cover. The projecting portion 202_1 and the engaging portion 204_1 are made of a conductive material to form a cover switch 205. When the projecting portion 202_1 and the engaging portion 204_1 are engaged with each other, an ON signal representing the engagement is transmitted from the cover switch 205 to the data processor. Therefore, in this arrangement, an operation signal representing that the cover clip 203 is unfastened is output as an OFF signal of the cover switch 205 when the projecting portion 202_1 and the engaging portion 204_1 are disengaged from each other.

Fig. 18 shows a clock signal transmitter for transmitting a clock signal when the operation signal is output from the cover switch 205, and Figs. 19(a) to 19(j) show signal waveforms of the respective sections of the transmitter. The state of the cover switch is periodically monitored during an operation of a CPU (not shown) by software interruption. First, when the cover switch (represented by CV.SW in Figs. 18 and 19(f)) is opened at a timing t0 as shown in Fig. 19(f), the ground potential supplied to a terminal 212 is stopped, and the terminal 212 goes to level "1". This signal is supplied as a CV.ST signal to a terminal 228 and periodically monitored by the CPU. When a power switch 219 is depressed at a timing t1, the ground potential is supplied to the input terminal of an inverter 222, a signal of the inverter 222 goes to level "0" as shown in Fig. 19(e). Therefore, since both input terminals of an AND gate 223 go to level "1", a flip-flop 224 fetches a signal of level "1" from the D input terminal and outputs the signal of level "1" from the Q output terminal. As a result, a signal shown in Fig. 19(g) is output from an NMI (non maskable interrupt) terminal 226. Since this NMI signal is also supplied to an oscillator 217 via an OR gate 216, the oscillator 217 is set in a clock enable (CLK.EN) state as shown in Fig. 19(a) to generate a clock signal CLK having a frequency determined by an oscillating member 218. Therefore, a clock (CLK) signal is output from a terminal 225 as shown in Fig. 19(b).

At the same time the clock is supplied to cause the CPU to start its operation, interruption is generated by the signal NMI, and software recognizes that the cover is opened and a normal operation can be started. As a result, at a timing t2, the CPU (not shown) supplies a write signal $\overline{\text{REG.W}}$ shown in Fig. 19(c) to a terminal 211 and data signal CPU.DT to a terminal 210. The data signal CPU.DT of level "0" is supplied in order to generate the clock signal, and that of level "1" is supplied in order to stop the clock signal to set a sleep state. Since a timing t4 is a timing at which the operation of the apparatus is started, the clock signal must be intermittently generated. Therefore, the data CPU.DT is at level "0". For this reason, as shown in Fig. 19(d), a signal CLK.REG of level "0" is output from the Q terminal of the flip-flop 214. This CLK.REG signal is supplied to the oscillator 217 via the OR gate 216.

Since the CPU supplies a signal $\overline{\text{NMI.CL}}$ to a terminal 213 at a timing t4 as shown in Fig. 19(h), the signal NMI supplied from the flip-flop 224 goes to level "0" as shown in Fig. 19(g). Therefore, the oscillator 217 operates by only the signal CLK.REG supplied from the flip-flop 214.

When a power switch 219 is depressed in order to stop the apparatus operation at a timing t5, a signal of level "0" shown in Fig. 19(e) is supplied to the inverter 222, and a signal of level "1" is supplied from the flip-flop 224. Therefore, the signal NMI shown in Fig. 19(g) is supplied from a terminal 226. This NMI signal is supplied from the terminal 226 to the CPU. After the NMI interruption processing routine clears the NMI by the signal $\overline{\text{NMI.CL}}$ signal, the signal $\overline{\text{REG.W}}$ shown in Fig. 19(c) is supplied to the terminal 211 at a timing t7, and a signal of level "1" is supplied to the terminal 210. Therefore, since the flip-flop 224 fetches the signal of level "1" and outputs it from the Q terminal, the signal CLK.REG shown in Fig. 19(d) is supplied to the oscillator 217 via the OR gate 216. Since the signal NMI is not generated at a timing t8, the signal CLK.EN goes to level "0", thereby stopping the operation of the oscillator 217 and generation of the clock signal. Therefore, the signal CLK shown in Fig. 19(b) supplied from the terminal 225 is no longer supplied. When the clock signal is stopped as described above, the CPU stops its operation to reduce power consumption.

When the power switch 219 is depressed again at a timing t9, the clock signal is generated as described above. When the cover switch is closed at a timing t14, closing of the cover switch is detected at a timing t15 as a monitor timing since the state of the cover switch is periodically monitored by software interruption of the CPU as shown in Fig. 19(i). This detection result is supplied as a signal CV.ST from the terminal 228 to the CPU. Therefore, since the CPU supplies the signal $\overline{\text{REG.W}}$ to the terminal 211 and a signal of level "1" to the terminal 210, the signal CLK.REG goes to level "1" as shown in Fig. 19(d) to stop the clock signal. That is, the clock signal is stopped not only when the operation of the apparatus is stopped by the power switch but also when the cover switch is closed during the operation, thereby reducing the power consumption. Therefore, even if the power switch 219 is accidentally turned on while the apparatus is carried by a user, no clock is supplied to the CPU so as not to unnecessarily consume the power.

Figs. 20 and 21 show flow charts of operations of the CPU. NMI interruption processing shown in Fig. 20 is performed each time the signal NMI is generated. Referring to Fig. 20, if the CPU determines in step 300 that the switch state, i.e., SW.ST of the terminal 227 is at level "1", the CPU checks in step 301

whether currently ON, i.e., whether the power source is switched on for the first time. Since "NO" is determined in an initial state, power flag ON processing, processing for switching the signal CLK.REG to level "0", and NMI clear processing are performed in steps 302 to 304, and the flow returns to a normal processing routine in step 305.

When the power source is switched on, i.e., when the clock signal is generated, power flag OFF processing, NMI clear processing, and processing for switching the signal CLK.REG to level "1" are performed in steps 306 to 308. If the switch state is not 1 in step 300, other NMI processing is performed in step 309.

Fig. 21 shows software interruption processing. Referring to Fig. 21, in step 310, whether the cover switch is open is monitored by software interruption. If the cover switch is not open, power flag OFF processing and processing for switching the signal CLK.REG to level "1" are performed in steps 311 and 312. If the cover switch is open, other periodic interruption is performed in step 313.

Figs. 22 and 23 are circuit diagrams showing other embodiments of the present invention, in which control for generating or stopping a clock signal is not performed but a power source current is directly controlled. In this case, a main body switch 161 and a cover switch 135 must be normally ON. That is, once the main body switch 161 or the cover switch 135 is set in an ON or OFF state, it must be continuously in the ON or OFF state until the state changes next. Referring to Fig. 22, the power switch 161 of the main body and the cover switch 135 are connected in series with each other, and a current is supplied from a battery 160 to a load 162 when both the switches are closed. Referring to Fig. 23, when the cover switch 135 is turned on, a signal of level "1" is supplied from the battery 160 to a buffer via a resistor 163, thereby turning on a transistor 165. Therefore, when a power switch (a power source switch at the main body side) is in an ON state, a transistor 166 is also in an ON state to supply a current to the load 162.

Figs. 24(a) and 24(b) show another embodiment of the cover switch, in which a cover clip 133 is fastened by a clip fastener 170. When the cover clip 133 is fastened by the clip fastener 170, contacts 171 and 172 are brought into contact with each other.

Figs. 25(a) and 25(b) show still another embodiment of the cover switch comprising a push button switch 180 at the cover side. When a cover clip 133 is open, the push button switch 180 is in a state shown in Fig. 25(a). When the cover clip 133 is closed, the push button switch 180 is pushed and turned on by a projecting portion 181. At this time, the projecting portion 181 is engaged with engaging pins 182 and 183 so as not to be removed.

Fig. 26 shows an embodiment of the present invention. Referring to Fig. 26, reference numeral 251 is an expansion card holder having rings 251_1 for holding paper and a releasing metal piece 251_2 for opening the rings 251_1. Engaging portions 251_3 are formed at two ends in the longitudinal direction of the expansion card holder 251. The engaging portions 251_3 are engaged with portions 252_1 and 253_1 to be engaged of electronic processors 252 and 253, respectively, thereby pivotally engaging the electronic processors 252 and 253.

A battery holder 254 is fitted in the rear surface of the expansion card holder 251. Fig. 27 shows the battery holder 254 in detail. Referring to Fig. 27, a cover 254_1 can be opened to replace a battery in the holder 254. Fig. 28 shows a battery 255 to be used in this apparatus. Connectors 254_2 and 254_3 having a predetermined number of electrodes are formed at two end portions in the longitudinal direction on a fitting surface, i.e., at the expansion card holder side of the battery holder 254 and electrically connected to connectors 252_2 and 253_2 of the electronic processors 252 and 253, respectively.

Referring to Fig. 26, the expansion card holder 251 is fitted in the connectors 254_2 and 254_3 of the battery holder 254 and is fitted in the battery holder 254. The portions 252_1 and 253_1 to be engaged of the electronic processors 252 and 253, respectively, are engaged with the engaging portion 251_3 of the expansion card holder 251 so as to be pivoted, i.e., opened/closed. A soft cover 256 is detachably mounted on the rear surface of the battery holder 254.

The electronic processor 252 has data input keys, and the electronic processor 253 has a CPU, a RAM, and a ROM and mounts an expansion card or the like as needed.

In the apparatus having the above arrangement, since the battery holder 254 is detachable and fitted in the expansion card holder 251, a battery having a necessary capacity can be used. If a battery having a large capacity must be used, only the thickness of the battery holder 254 need be increased while its width is kept unchanged. In this case, although a larger cover 256 is required since the thickness of the battery holder 254 is increased, the cover 256 can be easily replaced. In addition, since the cover 256 has a degree of freedom to a certain extent, the cover 256 need not be replaced if it can house the battery holder within the range of the degree of freedom. The expansion card holder 251 can be replaced by a larger holder 251a as needed as shown in Fig. 29. This large paper holder 251a has the same width as that of the holder shown in Fig. 26. Instead, an engaging portion 251_{3a} is formed at the rear surface side (lower side) in

contact with both end portions, and the portions 252_1 and 253_1 to be engaged of the electronic processors 252 and 253, respectively, are engaged with the engaging portion 251_{3a}. Therefore, the thickness of the holder need not be increased.

Fig. 30 shows an embodiment of the present invention. In this embodiment, since a display unit 1_1 is of a touch panel type, a user can select a necessary screen by touching a predetermined portion in accordance with displayed instruction. Fig. 30 shows only a part of a keyboard. If only keyboards A, B, and C are necessary as shown in Fig. 30, only the necessary portions can be displayed to facilitate an operation. In the present invention, when a keyboard is displayed on the screen, a key code corresponding to the keyboard is directly output by touching a portion corresponding to the key. Fig. 31 shows a circuit for outputting a key code. This circuit is constituted by an arithmetic processor 1_{12}, a coordinate input unit 1_{13}, an input coordinate extracting means 1_{14}, a table 1_{15}, and a memory 1_{16}. The arithmetic processor 1_{12} receives a coordinate range designation signal and a key code extraction instruction.

The coordinate range designation signal is used to designate display contents to be displayed on the display unit 1_1. For example, the signal is used to display the ranges of keys A, B, C, D, and E as shown in Fig. 30. As shown in Fig. 30, the display unit 1_1 is divided into 50 coordinates of Ia to Xe. Since the keys are assigned assuming that each key is rectangular, the range of each key can be designated by its upper left and lower right coordinate values. The coordinates of the key A shown in Fig. 30 are (left-4, up-5) and (right-24, down-15). Although blocks can be arbitrarily defined, each block has a size of 10 in both the vertical and horizontal directions in Fig. 30. For example, the coordinates of a block IVd are (left-30, up-30) and (right-40, down-40). When a coordinate range is designated to set the keys A to E as shown in Fig. 30, two types of tables like Tables 1 and 2 below are formed.

Table 1

No.	Coordinate Range	Key	Search Order
(1)	(4, 5) : (24, 15)	A	5
(2)	(27, 7) : (36, 23)	B	4
(3)	(54, 14) : (92, 36)	C	3
(4)	(61, 22) : (68, 28)	D	2
(5)	(77, 7) : (87, 25)	E	1

Table 2

Block	Registration Key	Block	Registration Key
Ia	(1)		
Ib	(1)		
Ic	-		
Id	-	VIIe	-
Ie	-	VIIIa	(5)
IIa	(1)	VIIIb	(3), (5)
IIb	(1)	VIIIc	(3), (5)
IIc	-	VIIId	(3)
IId	-	VIIIe	(3)
IIe	-	IXa	-
IIIa	(1), (2)	IXb	(5)
IIIb	(1), (2)	IXc	(3), (5)
IIIc	(2)	IXd	(3), (5)
IIId	-	IXe	(3)
IIIe	-	Xa	-
IVa	(2)	Xb	-
IVb	(2)	Xc	(3)
IVc	(2)	Xd	(3)
IVd	-	Xe	-

Registered keys are searched in the table in accordance with the depressed coordinates, and the input key is determined by comparing ranges of only the registered keys in the table. When a certain portion is depressed, only a coordinate signal in the block is output. For example, when a block VIIIb is depressed and a coordinate point (75, 18) in the block is input, the block VIIIb is determined from the coordinate value. Therefore, it is determined from Table 2 that keys (3) and (5) are registered. By comparing this data with Table 1, it is determined that a key code E does not correspond to a coordinate range but a key code C corresponds to the coordinate range. Therefore, the key code C is output. The present invention is characterized in that a coordinate signal is not output unlike in a conventional system but a key code is directly output. That is, a depressed block is checked, keys registered in the depressed block are checked, a key code to be output is determined on the basis of the data, and the determined key code is directly output. Therefore, as compared with a conventional system in which a wide area is sequentially searched to detect coordinates of a depressed portion and the coordinates are converted into a key code, a depressed portion can be determined at a high speed.

In Fig. 30, the block corresponding to the key C overlaps the keys D and E. These portions, however, may be searched in accordance with a priority order as shown in Table 1 to sequentially determine key codes.

Fig. 32 shows another embodiment of the present invention. Referring to Fig. 32, upper and lower left corners of an expansion card 4 are obliquely cut, and a transmitter 4_1 and a receiver 4_3 are provided at portions of the cut portions corresponding to a central axis 4_2 of expansion card holding holes. A receiver 1_{20} and a transmitter 1_{21} are mounted on portions on the central axis of a main body 1 corresponding to the transmitter 4_1 and the receiver 4_3, respectively. In this embodiment, the receiver 1_{20} and the transmitter 4_1 at the main body side are nondirectional, and the transmitter 4_1 and the receiver 4_3 at the expansion card side are directional toward the receiver 1_{20} and the transmitter 1_{21}, respectively.

In the apparatus having the above arrangement, the transmitter 41 and the receiver 43 at the expansion card side are provided on the central axis of the holding holes, and the transmitter 1_{21} and the receiver 1_{20} are provided on the central axis of the main body. Therefore, even if a play is present within an allowable range of a holder when an expansion card is held, the directivity is not easily shifted as compared with a case in which the transmitters and the receivers are provided at other portions.

Although the upper left corner of the expansion card is cut in Fig. 32, its lower left corner may be cut. Alternatively, a V-shaped notch as indicated by a dotted line in Fig. 32 may be formed at any portion of the left side (in Fig. 32, the notch is formed substantially at the center of the left side), and a transmitter and a receiver may be provided at the notch. The transmitter or receiver portion need not be linearly formed as shown in Fig. 32. For example, the portion may be curved to form a projection as shown in Fig. 33(a). In this case, a transmission direction may be scattered to facilitate reception at the main body side. Furthermore, the portion may be curved to form a recess as shown in Fig. 33(b), thereby focusing energy with respect to a receiving element. In this case, an efficiency can be further increased by using a reflecting paint or a reflecting plate on a cut surface.

Fig. 34 shows still another embodiment of the present invention, in which a display unit 1_1 is illustrated. The display unit 1_1 is constituted by a display portion 1_{22} at the main body side and a display emphasizing portion 1_{23} detachable with respect to the display portion 1_{22}. The display portion at the main body side includes a touch panel 1_{22a} capable of inputting handwritten characters, a transmission display element 1_{22b} such as a liquid crystal, and a connecting portion 1_{22c}. The display emphasizing portion 1_{23} includes a light-emitting device 1_{23a}, a battery 1_{23b}, a connecting portion 1_{23c}, and a pawl 1_{23d} for engaging the display portion 1_{22} at the main body side with the display emphasizing portion 1_{23}. Referring to Fig. 34, the display emphasizing portion 1_{23} is removed from the display portion 1_{22}.

In the apparatus having the above arrangement, when the display portion 1_{22} is mounted on the display emphasizing portion 1_{23}, the connecting portions 1_{22c} and 1_{23c} are connected with each other, and illumination ON/OFF control is performed by a CPU at the main body side by using software via the connecting portions. Although the display emphasizing portion 1_{23} uses a light-emitting device, it may be a reflecting plate.

Since the display element of the display portion 1_{22} is of a transmission type, it can be used as an OHP sheet by removing the display emphasizing portion 1_{23}. In this case, since the display screen can be projected in an enlarged scale, a lot of people can see the screen at the same time.

Fig. 35 shows still another embodiment of the present invention. Referring to Fig. 35, when a display direction is designated by a display direction designating means 1_{2a}, this designation signal is supplied to a switching table 1_{2b} and a display switching means 1_{2d}. Therefore, a display signal having a switched direction is output from a display RAM 1_{2e} and supplied to and displayed on a display unit 1_{2f}. Therefore, regardless of whether a screen is vertically or horizontally set, a display direction can always be normal with respect to an operator by this holding method of the apparatus.

The switching table 1_{2b} stores key codes corresponding to display directions. The key codes are read out in accordance with the designation signal from the display direction designating means 1_{2a}. A direction key is depressed in a direction with respect to an operator. That is, in order to move a cursor upward, an operator depresses an upper portion of a cross direction key with respect to the operator. As a result, a signal corresponding to the position is output from the direction key, and a key code in a direction designated by the display direction designating means 1_{2a} is output from the switching table 1_{2b} as described above. Examples of the key code are as shown in Table 3.

Table 3

	Normal Key Direction			
Screen Direction	Up	Right	Down	Left
Normal	Up	Right	Down	Left
90° Right	Right	Down	Left	Up
Inverted	Down	Left	Up	Right
90° Left	Left	Up	Right	Down

That is, when the apparatus is used in a 90° -right state, i.e., when the apparatus is pivoted to the right through 90°, a graphic pattern displayed as indicated by a solid line in Fig. 36 is pivoted through 90° as indicated by a dotted line shown in Fig. 36. Therefore, in this 90° -right state, a key (represented by symbol B) of a cursor key 1_2 for moving the cursor to the left upon normal use is used to move it upward. Therefore, by changing functions of the cursor key 1_2 as shown in Table 3 in accordance with the direction of the screen, a user can always perform a key operation in accordance a physical position of the cursor key without paying any attention even if the direction of the screen is changed.

Fig. 37 shows an operation of the above apparatus, in which a predetermined table is selected in accordance with the direction.

Fig. 36 shows a detailed arrangement of the display direction designating means. Referring to Fig. 36, contact sensors are provided at the rear sides of hatched portions, and a designation signal is output from each sensor. That is, since a position held by a user is detected by the sensor, the direction of the screen is automatically determined on the basis of the signal. In this case, predetermined input keys are preferably provided at both the hatched portions for convenience.

Fig. 38 shows still another embodiment of the present invention, in which an electromagnetic induction coil is wound around central rings of rings 2_1 of an expansion card holder 2 so as to substantially cover the central rings. As shown in Fig. 39, this coil is independently wound around right and left rings, and their winding directions are set such that magnetic fields generated by the respective coils cumulatively act.

In this manner, a coil at the main body side is formed around the ring 2_1 of the expansion card holder 2, and air-core coils 4_5 inserted in holding holes of an expansion card 4 as shown in Fig. 40 are set to be perpendicular to the ring 2_1 as shown in Fig. 39 (in Fig. 39, only the air-core coil 4_5 of the expansion card is illustrated). Therefore, communication can be performed between the main body and the expansion card in a noncontact state.

Fig. 41 shows a circuit of a transmitting circuit and a receiving circuit for performing data transmission via the communicating means having the above arrangement. This circuit is characterized by a portion constituted by transistors Q1 and Q2, resistors R3 and R4, a diode D1, coils L1 and L2, and a capacitor C2. In order to transmit information by electromagnetic induction, it is preferred to flow a large current to a coil. This circuit, however, is designed to be driven by, e.g., a coin-type lithium battery which cannot generate a large current. If the battery is forced to generate a large current, quality of the battery is degraded. This problem is solved by setting the resistances and capacitance of the resistors R3 and R4 and the capacitor C2 at 270 Ω, 56 Ω, and 10,000 PF, respectively.

That is, the capacitor C2 is charged by a small current via the resistor R3 having 270 Ω to reduce a load of a battery. Upon discharge of the capacitor C2, a large current is flowed to the coil L1 via the resistor R4 having 56 Ω to generate a large magnetic field.

Signal transmission is performed via this circuit as shown in Fig. 42. That is, as shown in Fig. 42, a data pattern having 11 bits, i.e., one start bit of level "0", data bits D0 to D7, one parity bit, and a stop bit of level "1" is transmitted. Figs. 43(a) to 43(e) show how the respective bits are transmitted. That is, one bit shown in Fig. 43(a) is finely modulated as shown in Fig. 43(b), and this modulated wave is transmitted via the coil as shown in Fig. 43(c). At the receiving side, the transmitted wave is digital-converted as shown in Fig. 43-(d) and extracted as reception data as shown in Fig. 43(e).

A message format is as follows. That is, except for some messages, a basic message including both a message from the main body to the expansion card and that from the expansion card to the main body has a format of command -logic address - data string - message end - BCC. If no data string is present or a data length is fixed, the message end and the BCC are omitted. The BCC is an exclusive OR of all the data from the command to the message end.

As has been described above, the present invention comprises an expansion card holder mounted on a main body, a necessary number of expansion cards held by the holder, and a communicating means for transmitting/receiving data between the held expansion cards and the main body. Therefore, a necessary number of expansion cards can be used to realize simultaneous use of different types of data bases which cannot be performed by a conventional apparatus. Therefore, unlike in a conventional apparatus, since an expansion card need not be replaced to be used in accordance with the type of data base, a compact apparatus which can be easily used can be provided.

Claims

1. An electronic system pocketbook apparatus comprising:
a foldable and portable main body having functions of right and left portions coupled by a cover, folded

upon carrying of said main body so that said right portion overlaps the left portion, a folded portion being fastened by a cover clip provided to said cover, and having basic functions of controlling arithmetic operations and display data processing by using an internal controller, data inputting means, and displaying data on a display unit;

an expansion card holder mounted on said main body;

a necessary number of expansion cards held by said expansion card holder; and

communicating means for performing data transmission/reception between said held expansion cards and said main body via said expansion card holder.

2. An apparatus according to claim 1, wherein

said expansion card holder includes a first coil wound around said expansion card holder, and

said expansion card includes a second coil embedded in said expansion card and connected to said first coil by electromagnetic induction.

3. An apparatus according to claim 1, wherein optical transmitting/receiving means is arranged at a connecting portion between said expansion card and said expansion card holder.

4. An apparatus according to claim 3, wherein said optical transmitting/receiving means is infrared transmitting/receiving means.

5. An apparatus according to claim 1, further comprising a touch panel.

6. An apparatus according to claim 5, wherein said touch panel is also used as said display unit.

7. An apparatus according to claim 5, further comprising:

determining means for determining information writing when an area of a portion in contact with said touch panel is not more than a certain area, and determining information erasing when said portion is not less than the certain area; and

a controller for performing control in accordance with a determination result of said determining means.

8. An apparatus according to claim 1, wherein said controller includes cursor direction switching means for causing a cursor moving direction to coincide with a direction designated by a cursor moving direction designation key when a direction of said apparatus main body is changed.

9. An apparatus according to claim 8, wherein said cursor direction switching means includes a cursor key pad capable of rotating parallel to a mounting surface.

10. An apparatus according to claim 8, wherein said cursor direction switching means includes:

first reading means for reading out, in accordance with a signal from said display direction designating means, a key code according to a display direction from a memory for storing a key code for each direction; and

a cursor moving direction control circuit for controlling the moving direction of said cursor in accordance with the readout key code.

11. An apparatus according to claim 1, wherein said controller includes:

closing release detecting means for detecting that closing of said expansion card holder is released; and

operation stopping means for stopping an operation of each section when a signal is output from said closing release detecting means.

12. An apparatus according to claim 11, wherein said controller includes operation restarting means for restarting communication and the stopped operation of each section when said expansion card holder is closed after closing release.

13. An apparatus according to claim 12, wherein said expansion card receives power from said main body.

14. An apparatus according to claim 13, wherein said controller includes:

power interrupting means for interrupting the power supplied to said expansion card in accordance with an output from said closing release detecting means; and

operation stopping means for stopping an operation of each section after the power is stopped.

15. An apparatus according to claim 1, further comprising:

a cover switch for outputting, when said cover clip is removed, an operation signal indicating removal; and

a clock signal transmitting circuit for transmitting, when the operation signal is output from said cover switch, a clock signal for operating said controller.

16. An apparatus according to claim 1, further comprising a power source.

17. An apparatus according to claim 16, further comprising a power source forming circuit for forming a supply path of a power source current when the operation signal is output from said cover switch.

18. An apparatus according to claim 16, further comprising:

an expansion card holder having a plurality of engaging portions at two end portions in the longitudinal direction thereof or a lower portion in contact with said two end portions;

a battery holder to be fitted in a rear surface of said expansion card holder;

a connector provided at two end portions in the longitudinal direction at a fitting surface side of said battery holder with respect to said expansion card holder and having a predetermined number of electrodes;
a first electronic processor having a portion to be engaged with one of said engaging portions of said expansion card holder and a connector to be fitted in one of said connectors of said battery holder;
a second electronic processor having a portion to be engaged with the other engaging portion of said expansion card holder and a connector to be fitted in the other connector of said battery holder; and
a cover to be mounted on a rear surface side of said battery holder.

19. An apparatus according to claim 5, wherein when a screen display range designation signal is supplied, an image corresponding to the signal is displayed.

20. An apparatus according to claim 19, further comprising:
means for displaying a selection key having a range to be designated by the display range designation signal;
means for outputting a key code corresponding to the display range designation signal from data in a memory for storing key codes of all input keys; and
key code selecting means for outputting a key code selected from a screen by an operator from key codes selected in correspondence with the display range designation signal.

21. An apparatus according to claim 20, wherein said display unit is divided into a plurality of blocks.

22. An apparatus according to claim 21, wherein each of said blocks includes:
a first memory for storing a key name corresponding to said block; and
a second memory for storing a key code corresponding to coordinates on said display unit.

23. An apparatus according to claim 22, further comprising:
block detecting means for detecting a touched block;
first reading means for reading out a key name registered in said detected block by referring to said first memory; and
second reading means for reading out a key code corresponding to the readout key name by referring to said second memory.

24. An apparatus according to claim 1, further comprising:
expansion card side transmitting/receiving means mounted on a holder side portion of said expansion card to have oblique directivity; and
main body side transmitting/receiving means, provided near a central axis of an inner rear surface of said main body, for performing communication with respect to said expansion card side transmitting/receiving means.

25. An apparatus according to claim 1, wherein said display unit is a transmission liquid crystal.

26. An apparatus according to claim 25, wherein light passes through said apparatus at least at a display portion of said display unit.

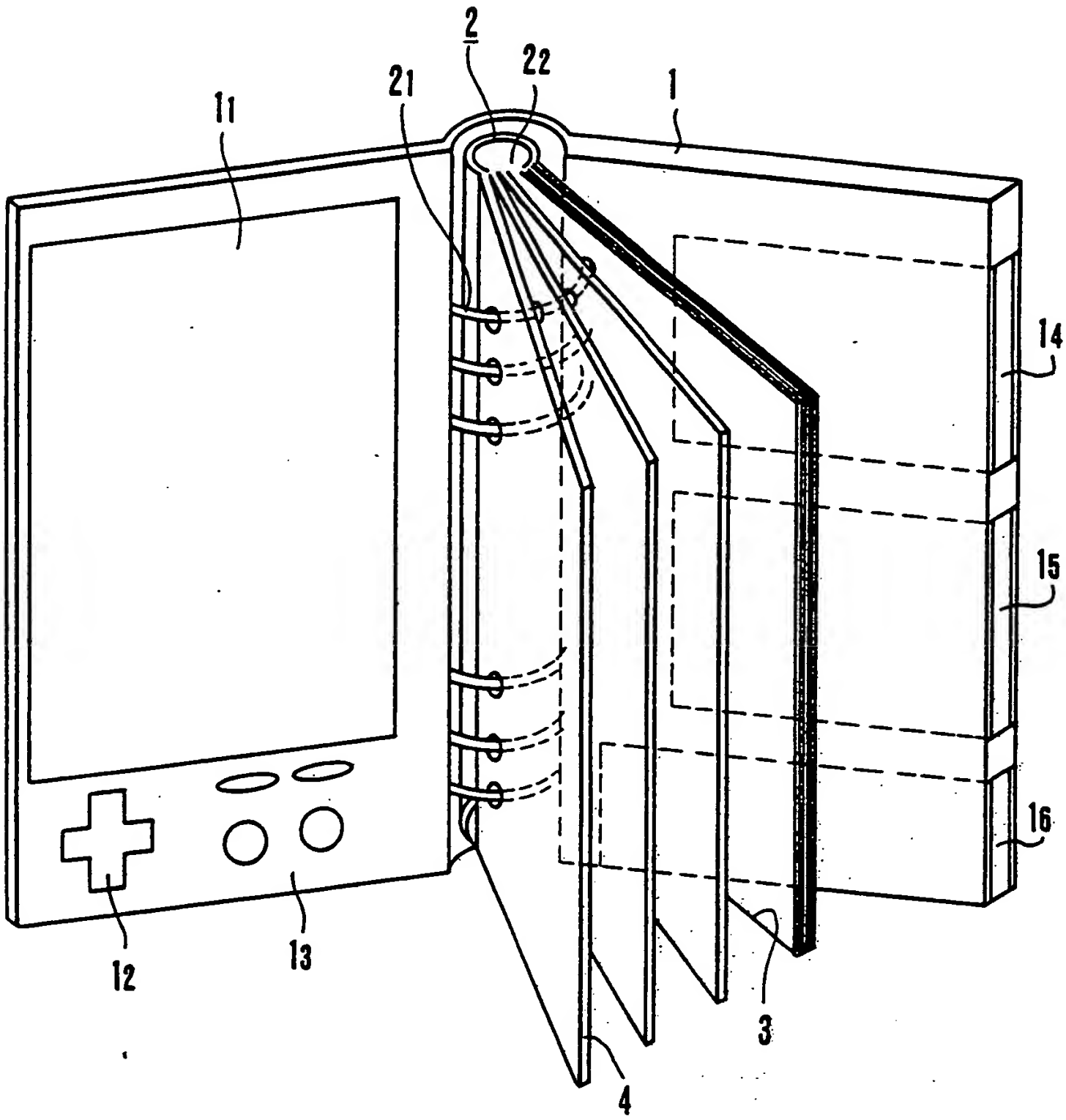


FIG.1

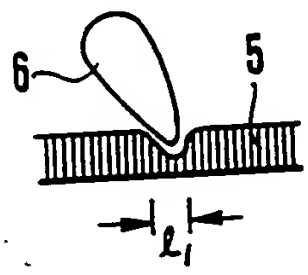


FIG.2(a)

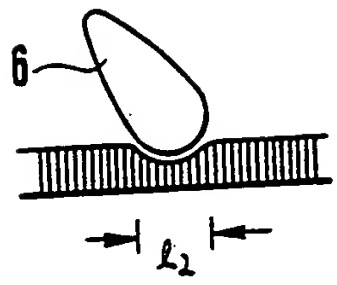


FIG.2(b)

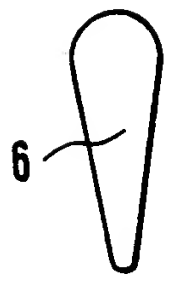


FIG.2(c)

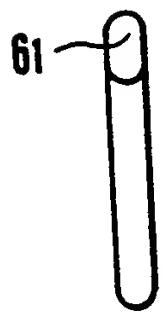


FIG.2(d)

FIG.2(e)

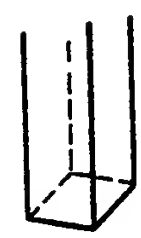


FIG.2(f)

FIG.2(g)

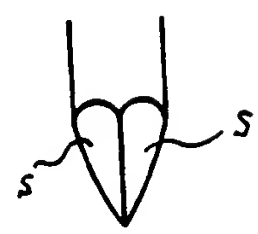


FIG.2(h)

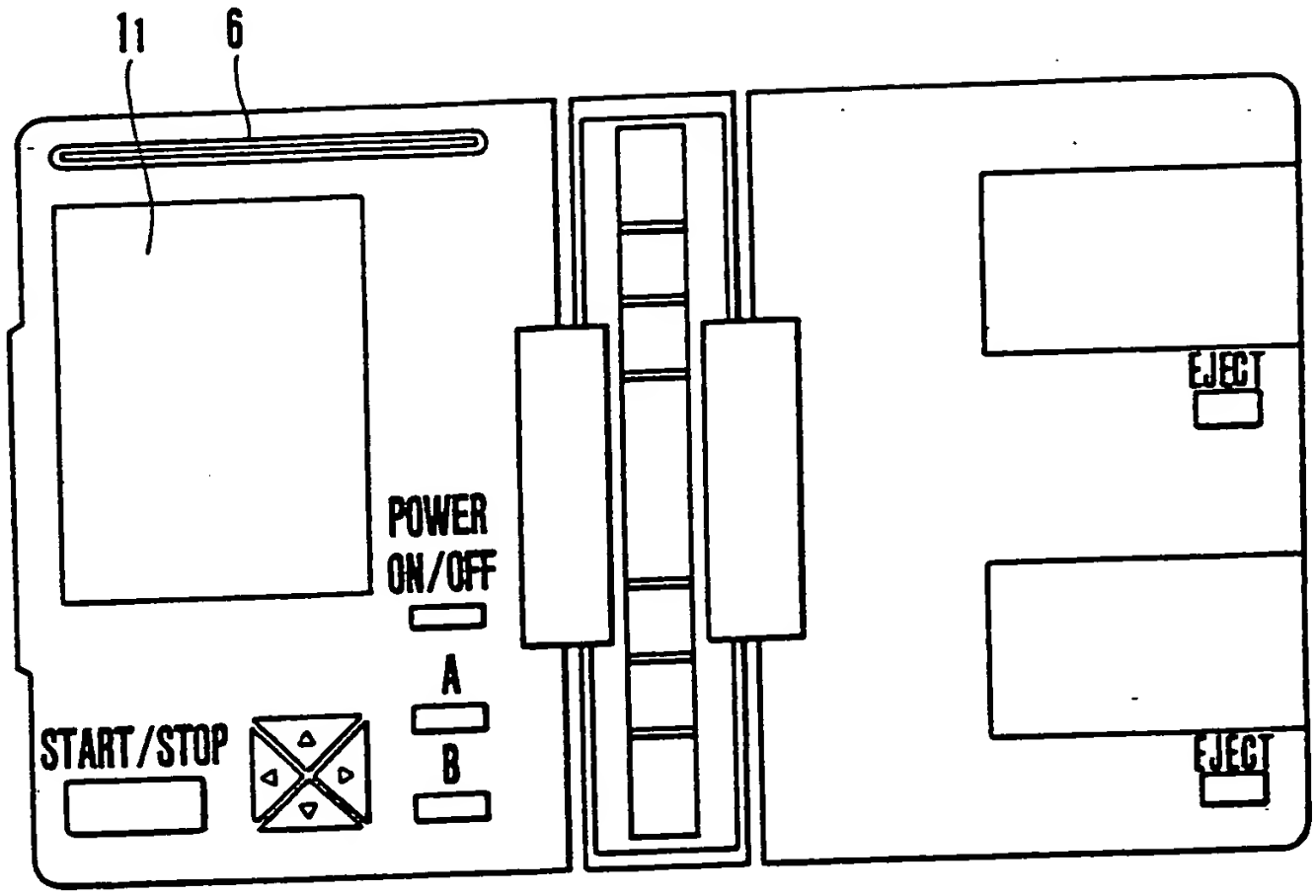


FIG.3

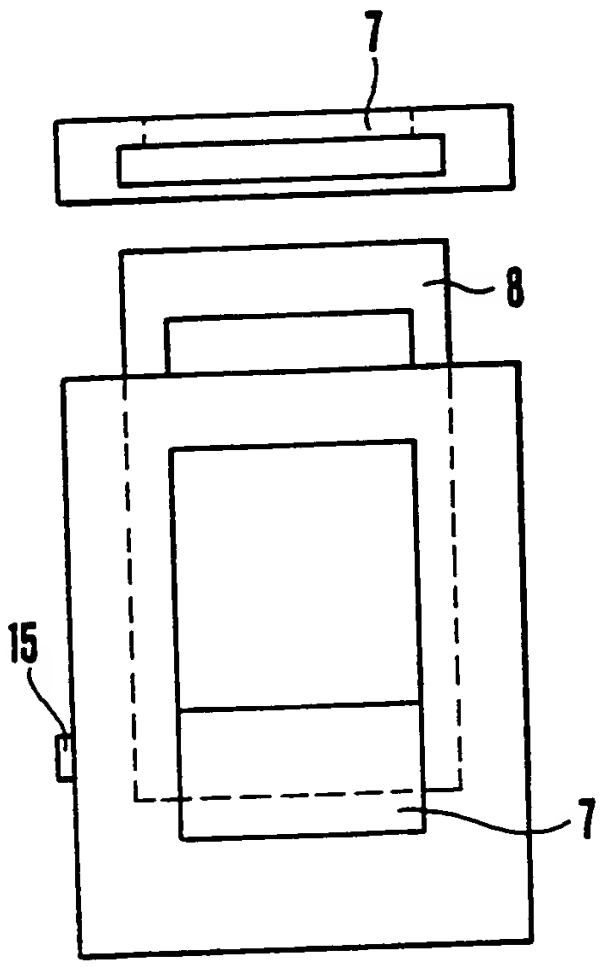


FIG.4

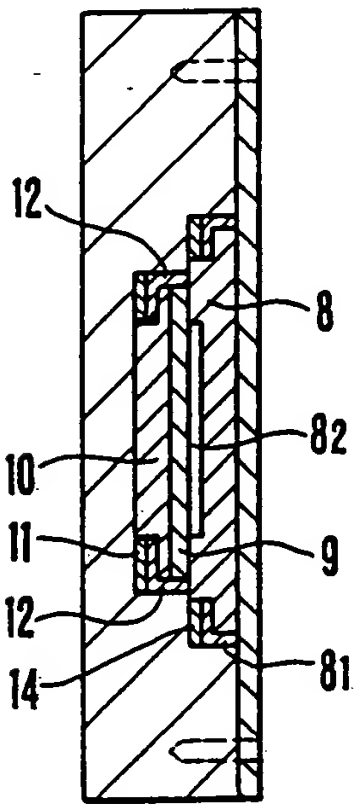


FIG.5(a)

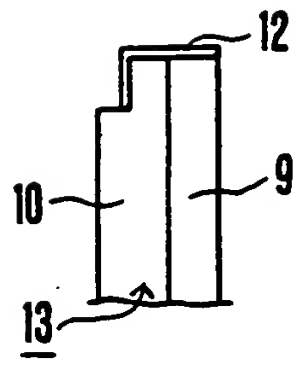


FIG.5(b)

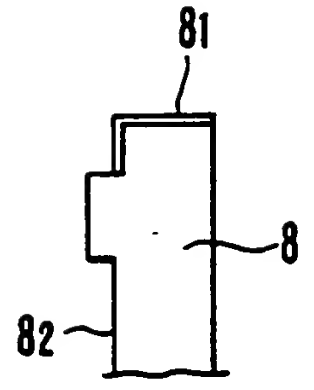


FIG.5(c)

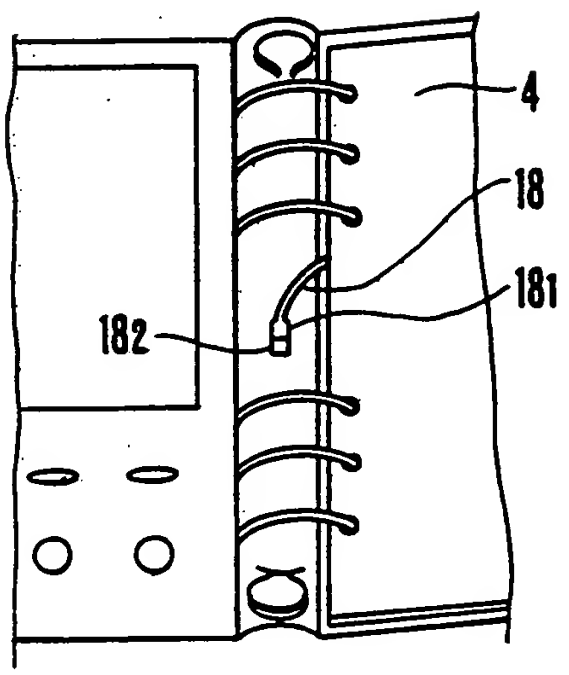


FIG.6

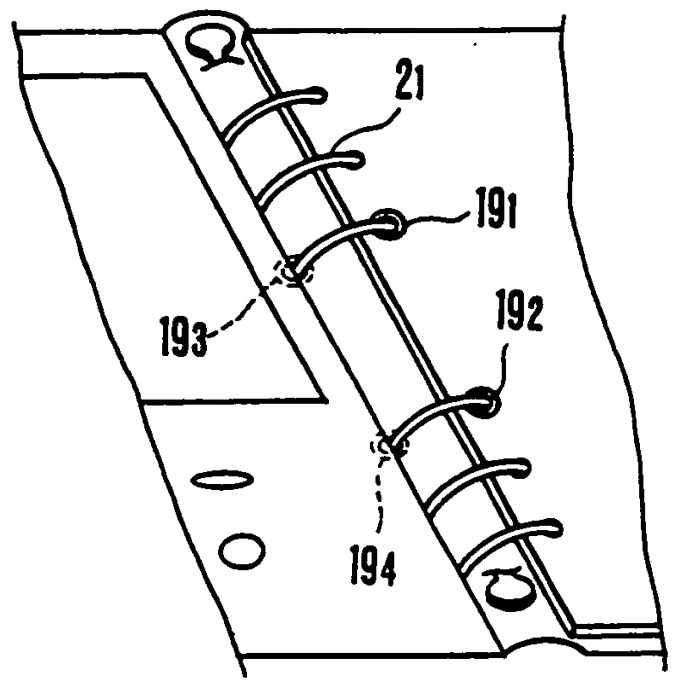


FIG.7

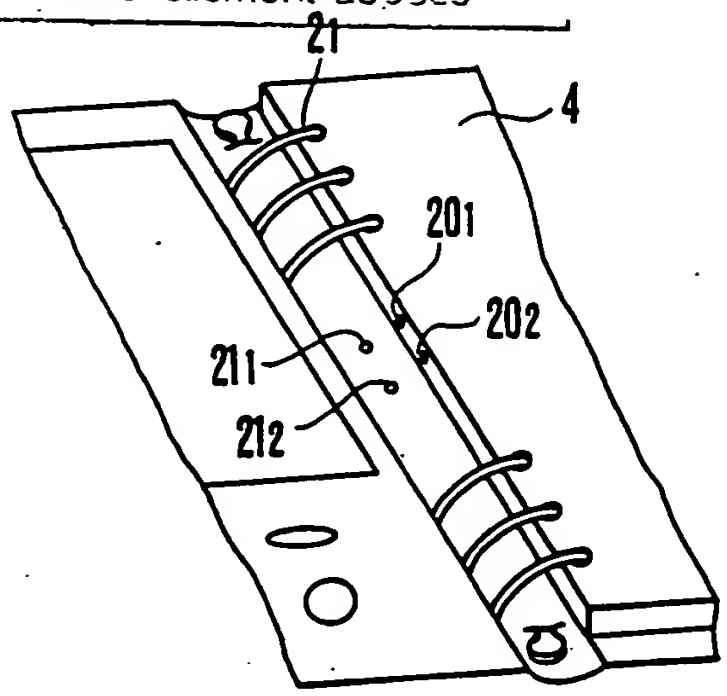


FIG.8

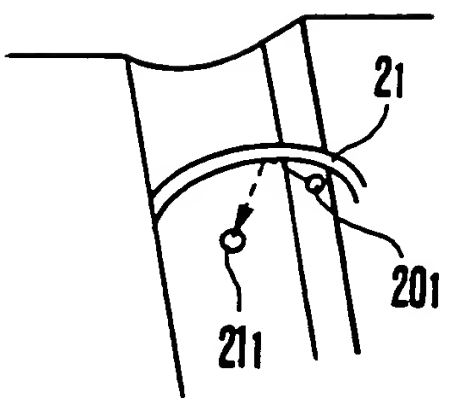


FIG.9

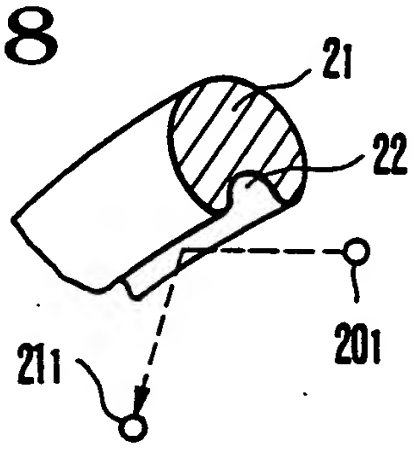


FIG.10

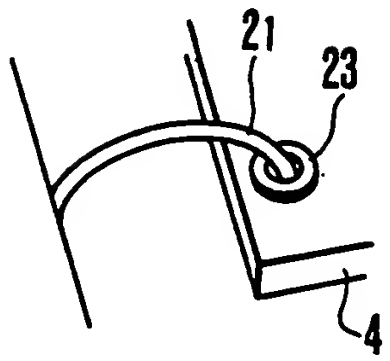


FIG.11

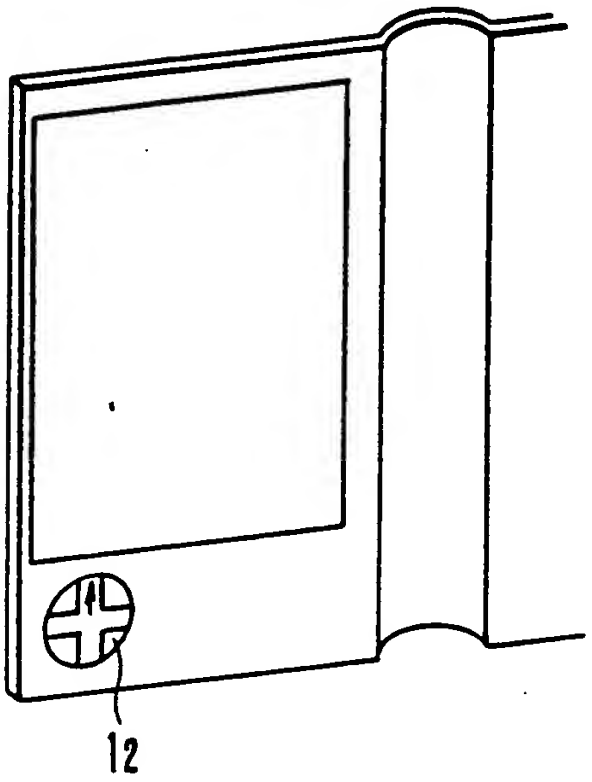


FIG.12(a)

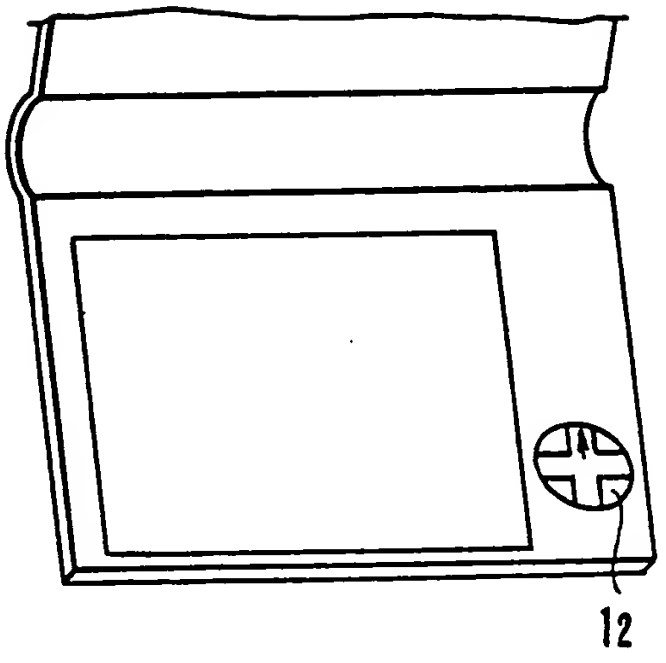


FIG.12(b)

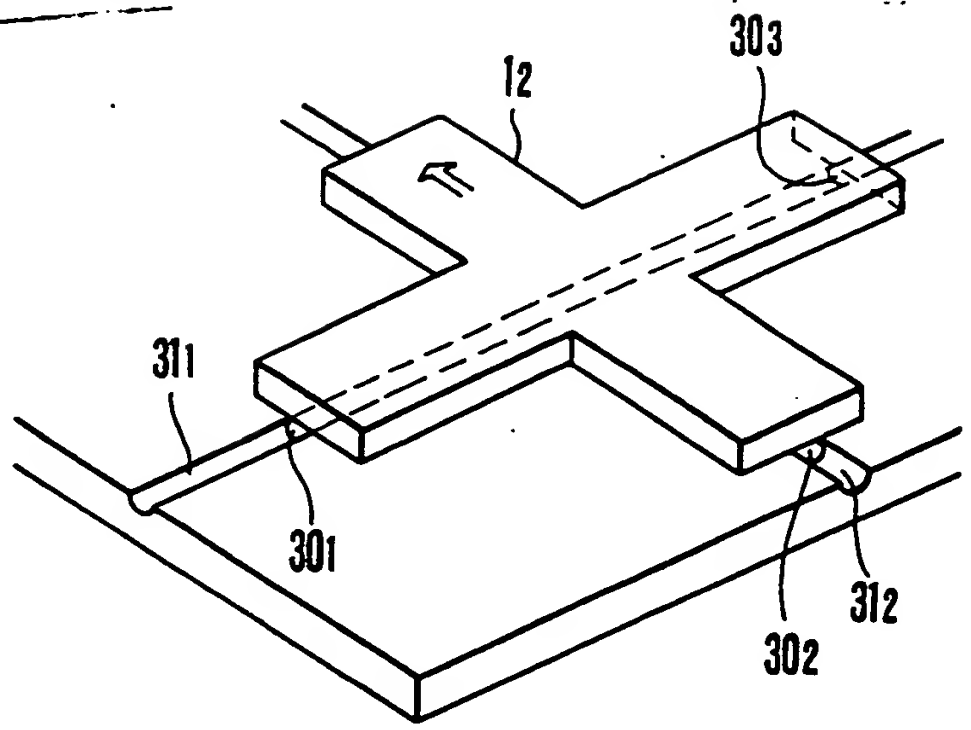


FIG.13

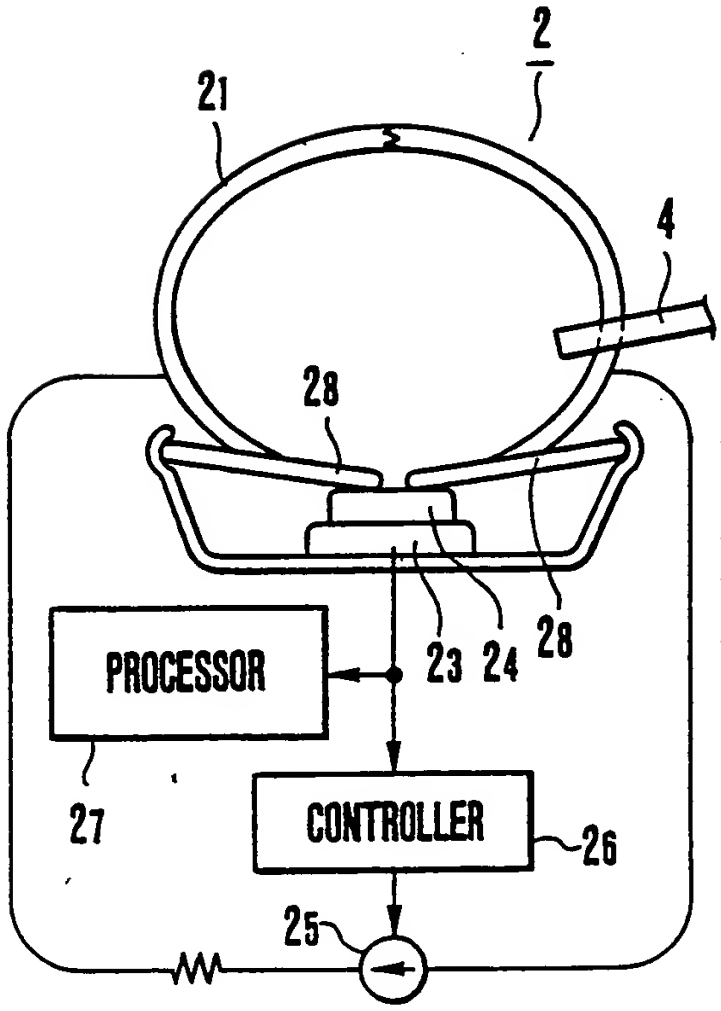


FIG.14(a)

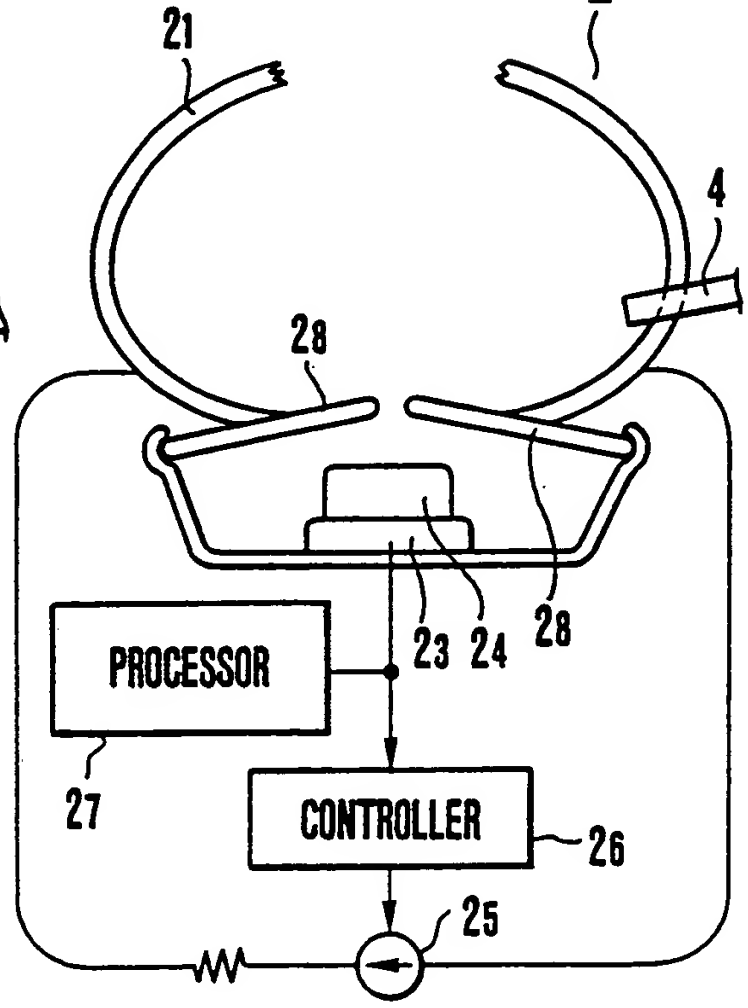


FIG.14(b)

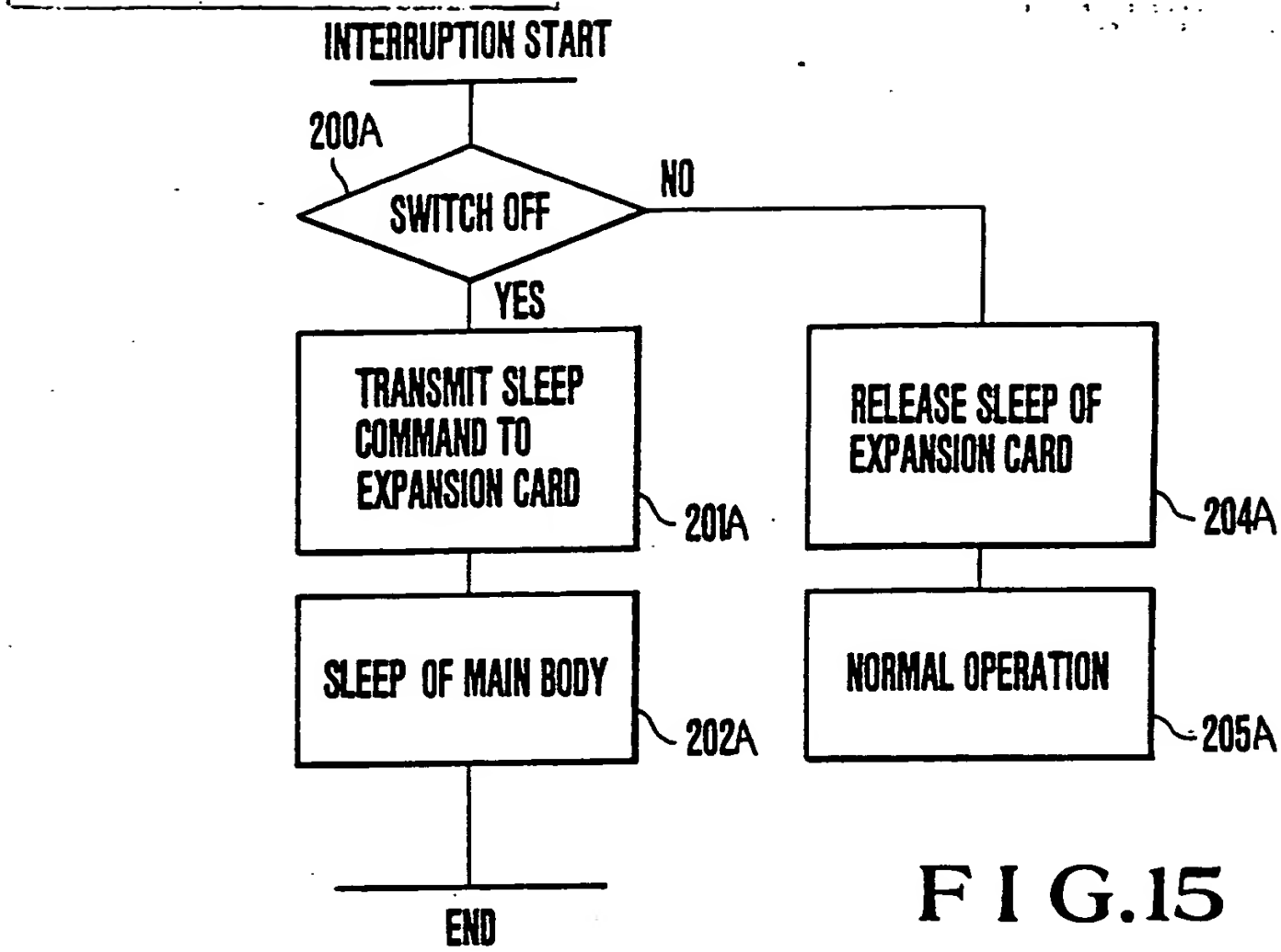


FIG.15

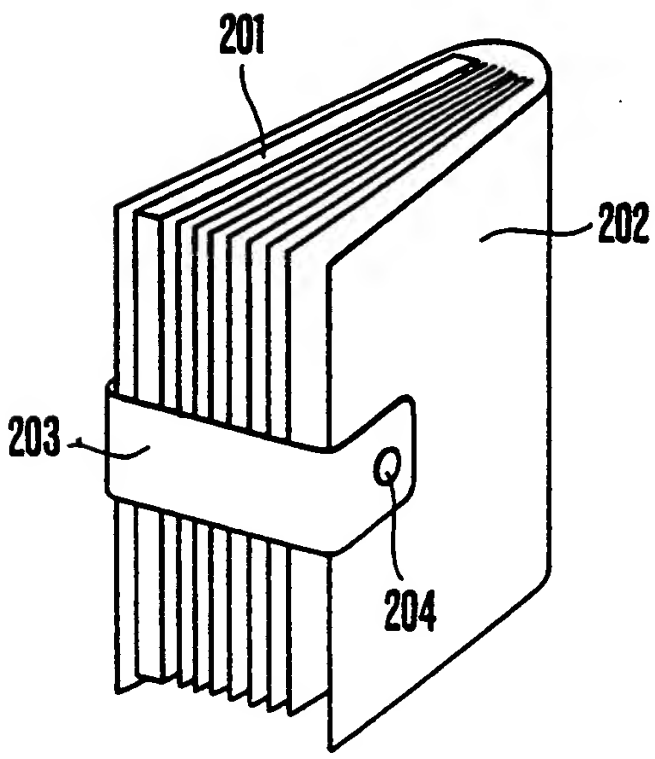


FIG.16

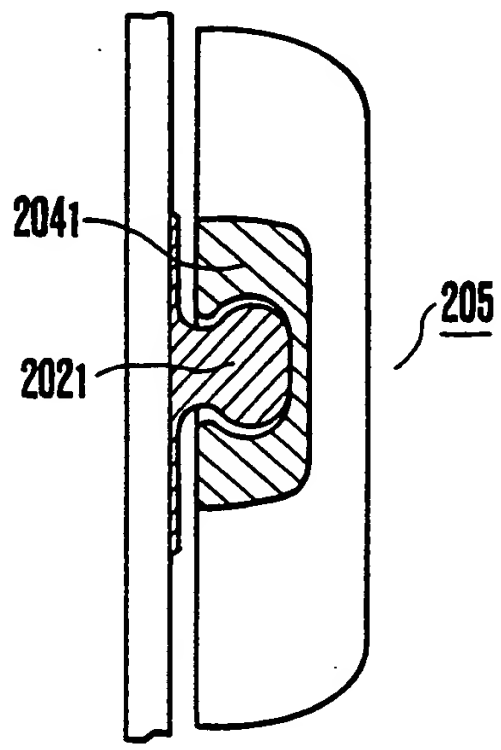
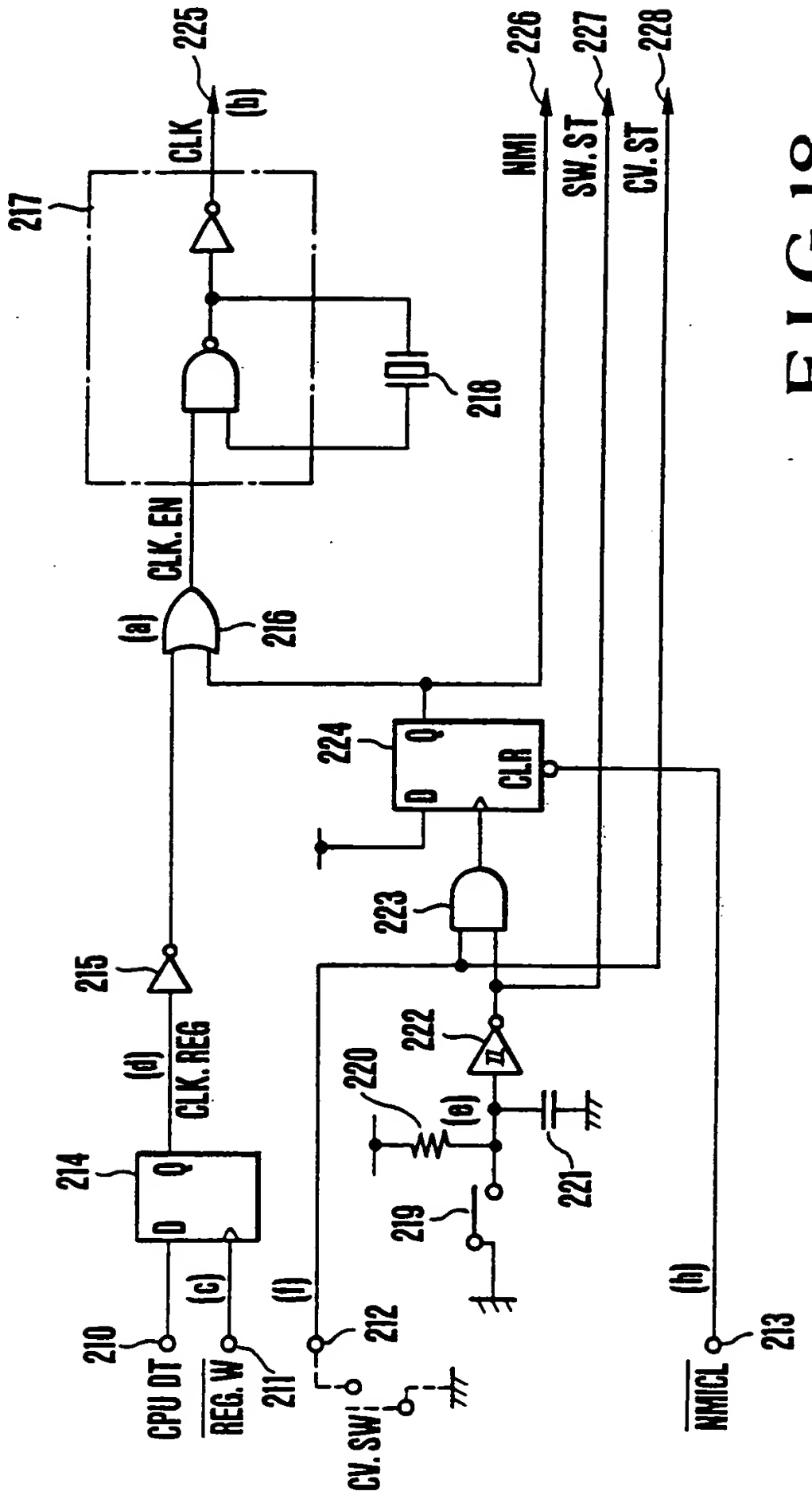


FIG.17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217
226
NMI
227
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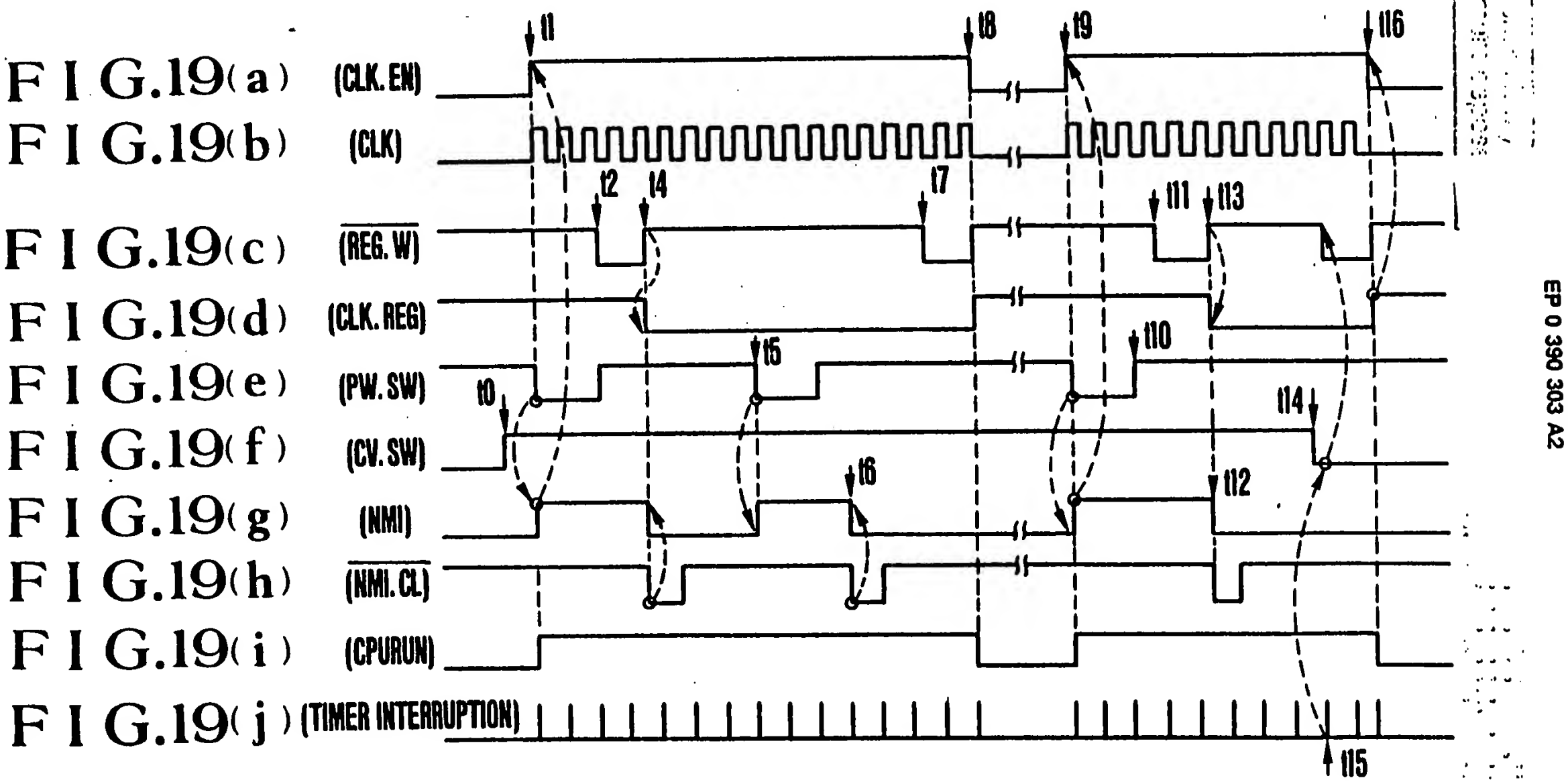
228
CV.ST
218
CLK.EN
(a)
216
224
D
Q
CLR
223
215
(d)
CLK.REG
222
220
(e)
214
D
Q
219
221
(c)
(f)
210
CPU DT
REG.W
211
212
CV.SW
(h)
NMICL
213

FIG.18



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